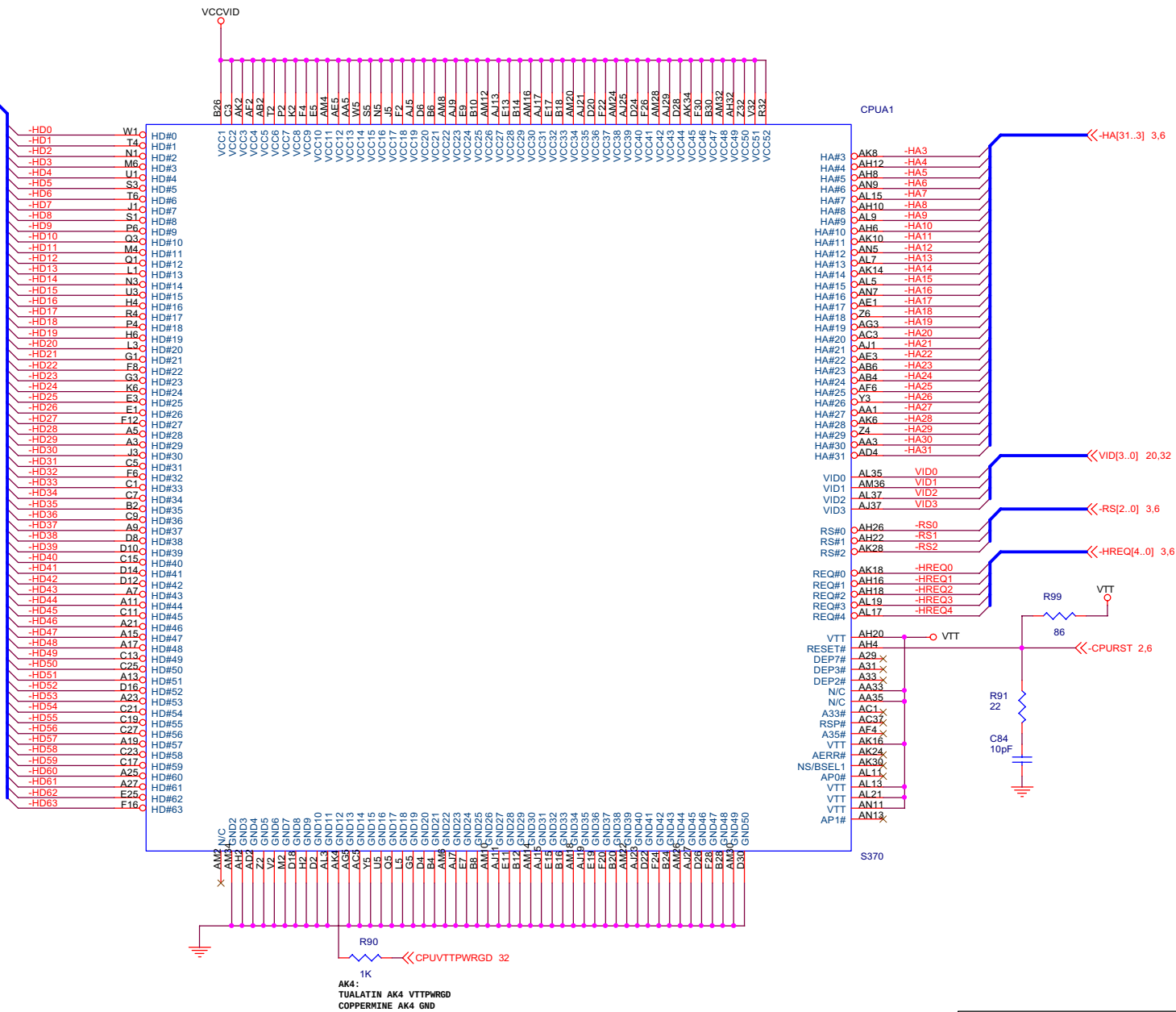
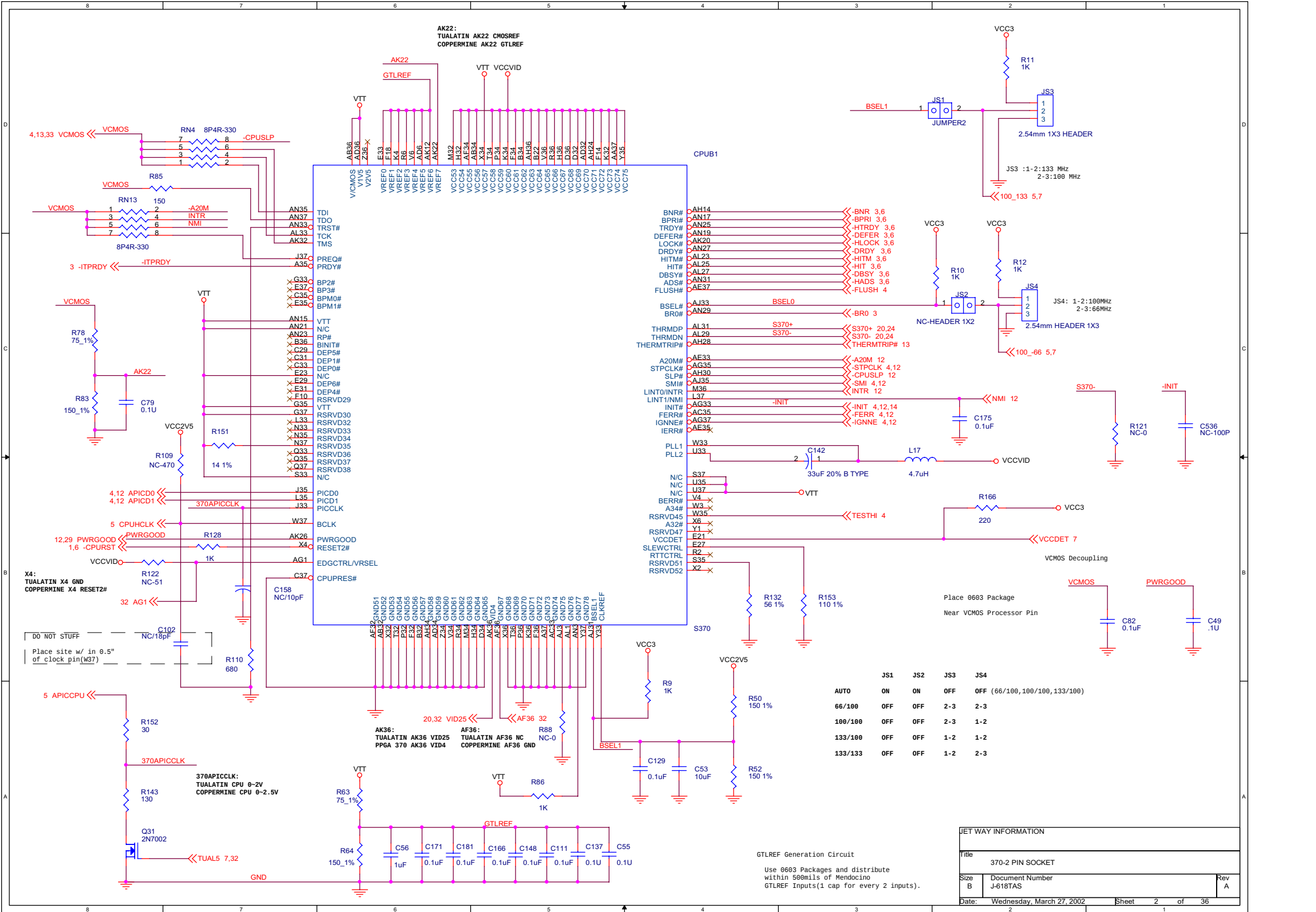


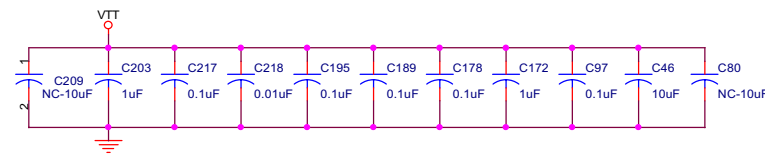
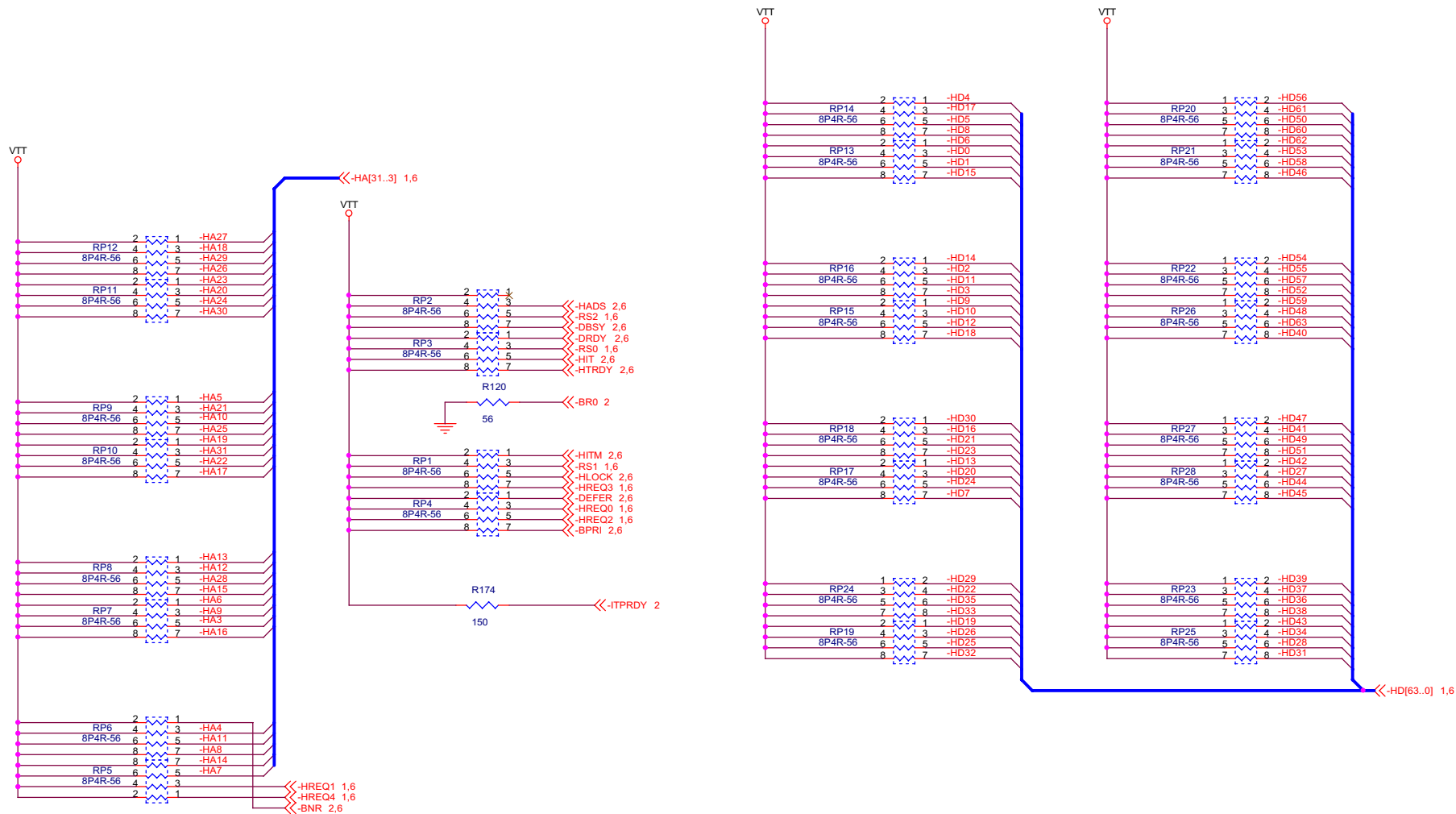
J618TAS

1. LINK
2. SCH
3. SCH
4. SCH
5. SCH
6. SCH
7. SCH
8. SCH
9. SCH
10. SCH
11. SCH
12. SCH
13. SCH
14. SCH
15. SCH
16. SCH
17. SCH
18. SCH
19. SCH
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22. SCH
23. SCH
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27. SCH
28. SCH
29. SCH
30. SCH
31. SCH
32. SCH
33. SCH

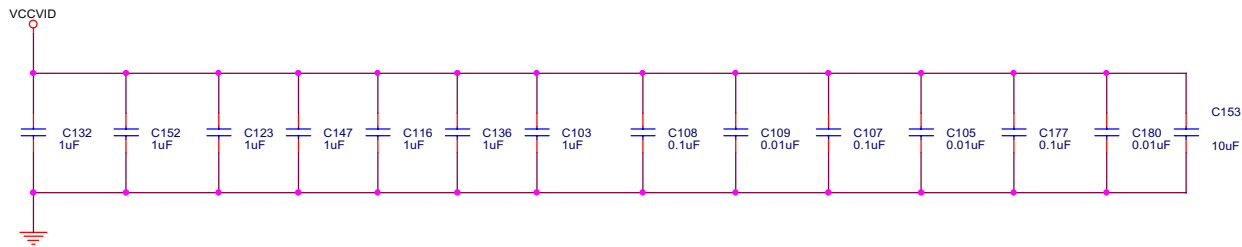


JET WAY INFORMATION			
Title			
370-1 PIN SOCKET			
Size	Document Number	Rev	
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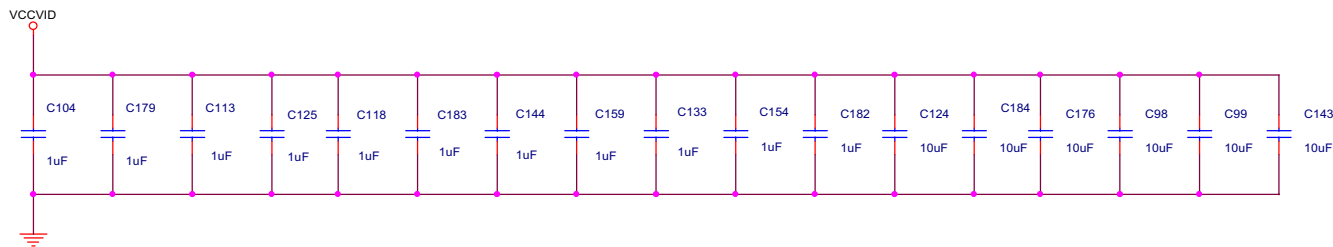




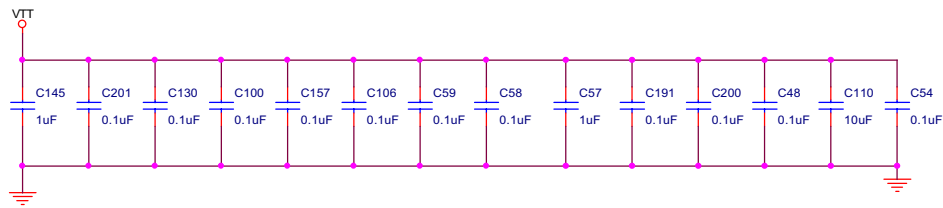
JET WAY INFORMATION			
Title			
GTL Termination			
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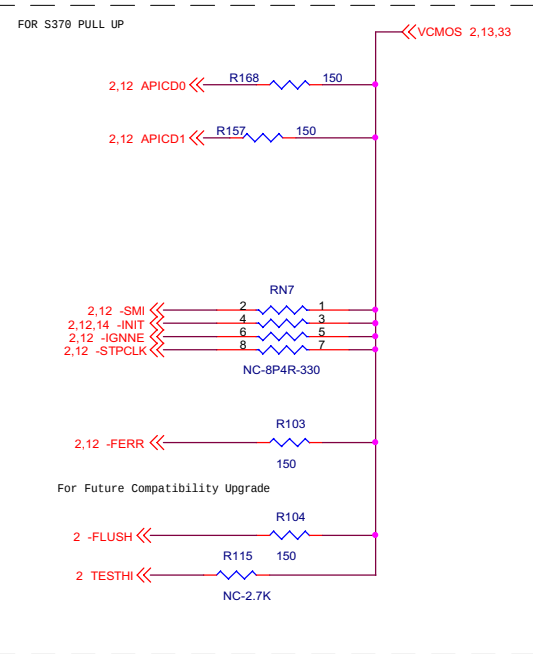
FOR CPU



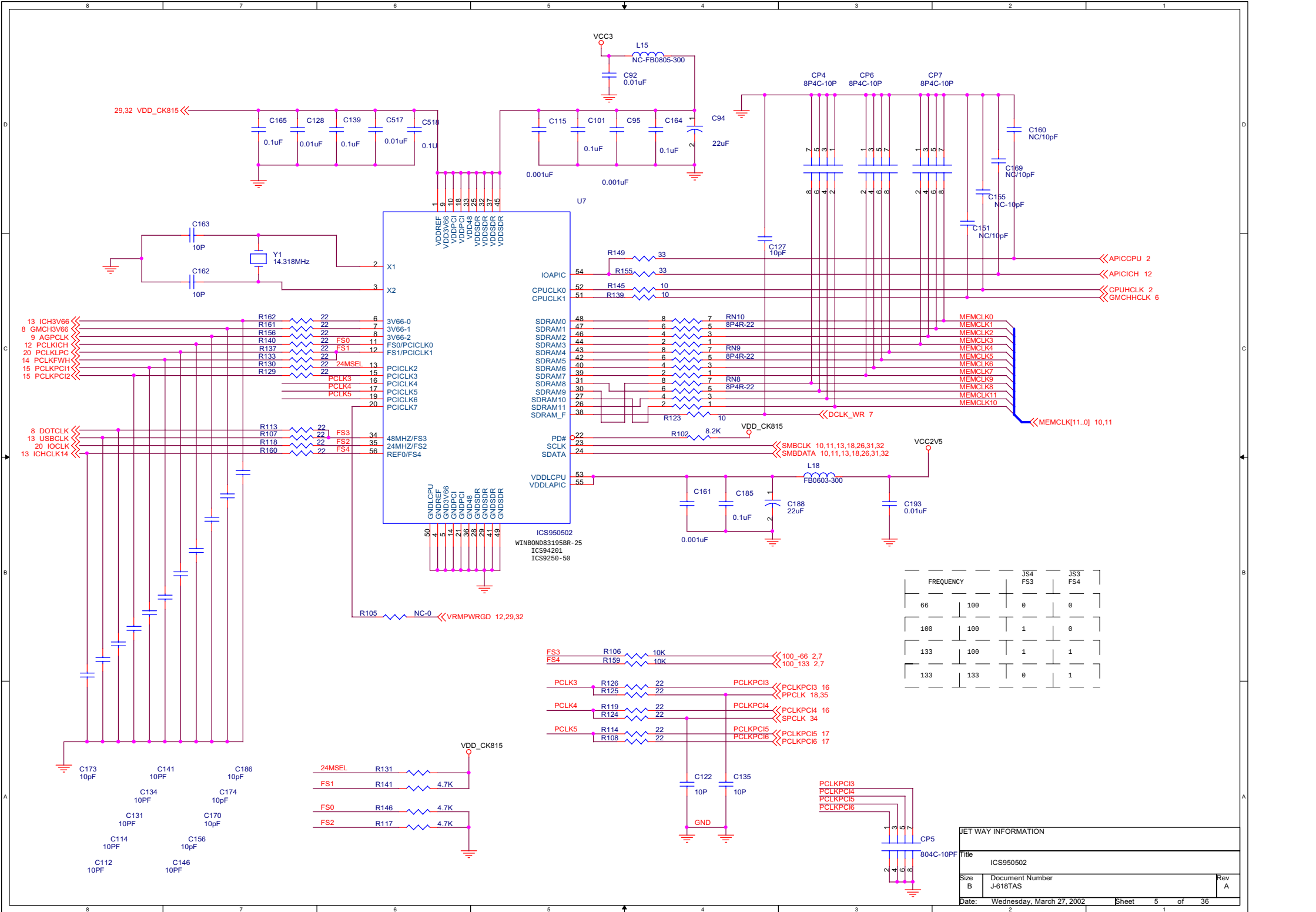
FOR CPU

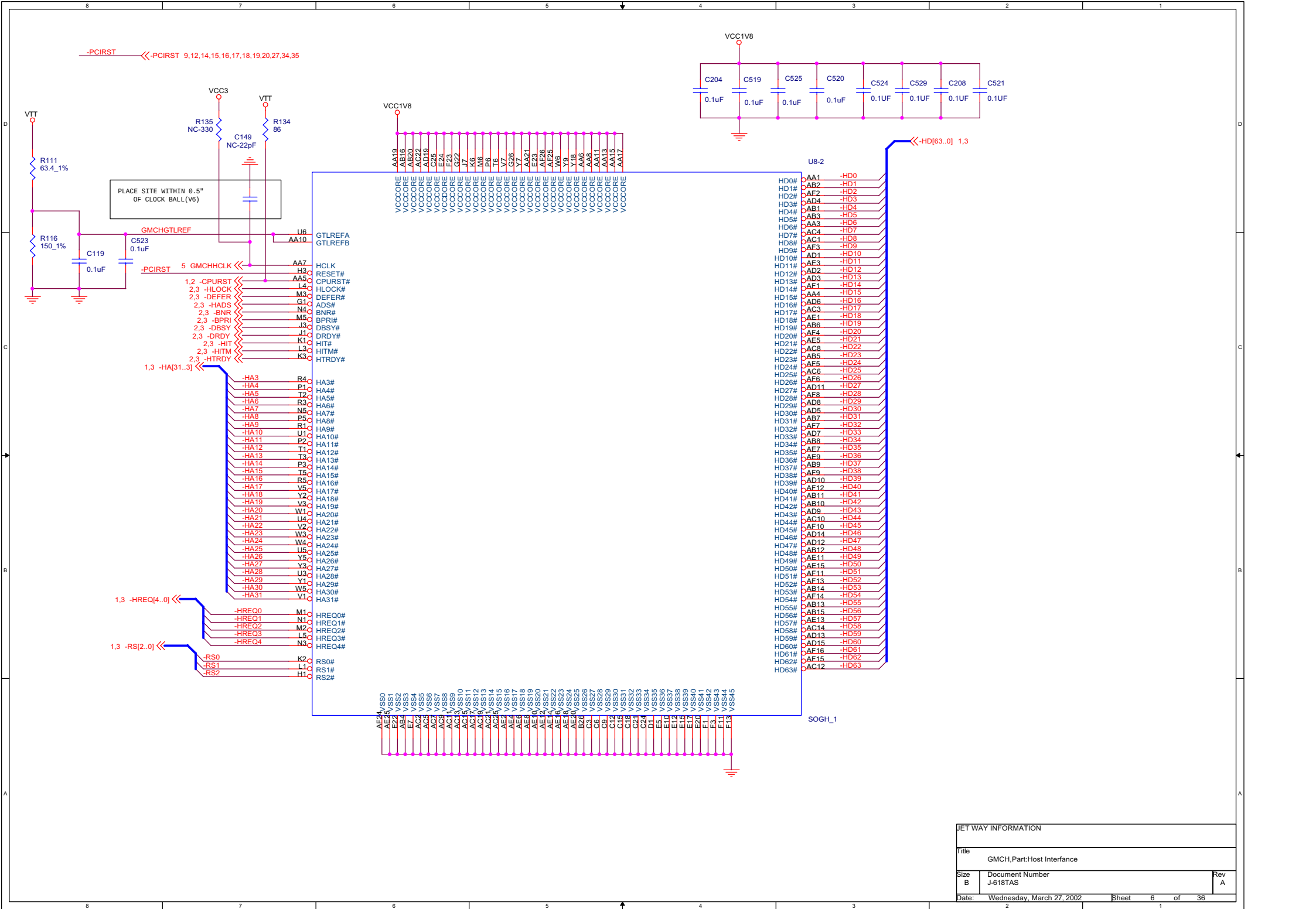


FOR CPU VTT

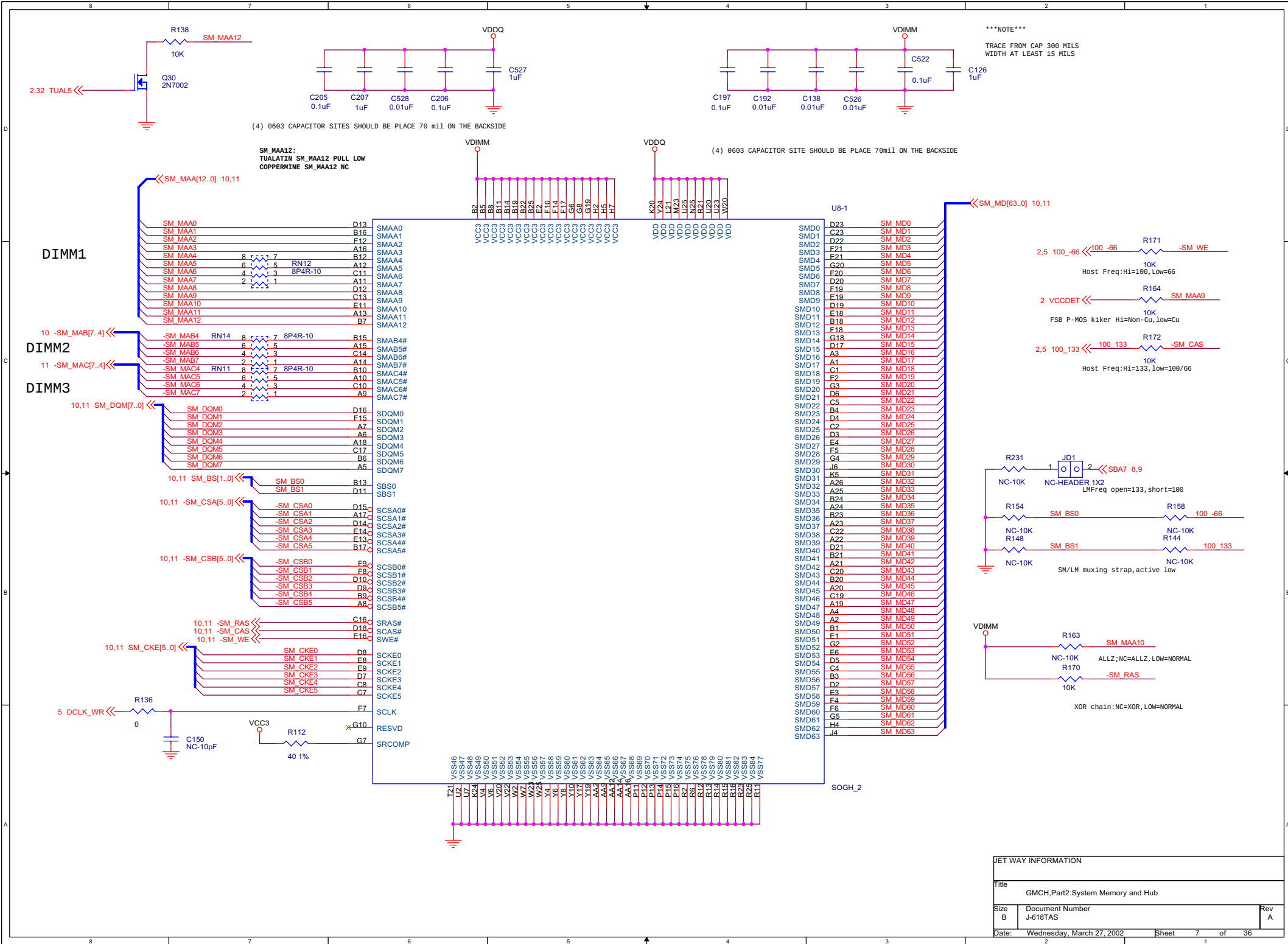


JET WAY INFORMATION			
Title			
370-pin Socket Decoupling			
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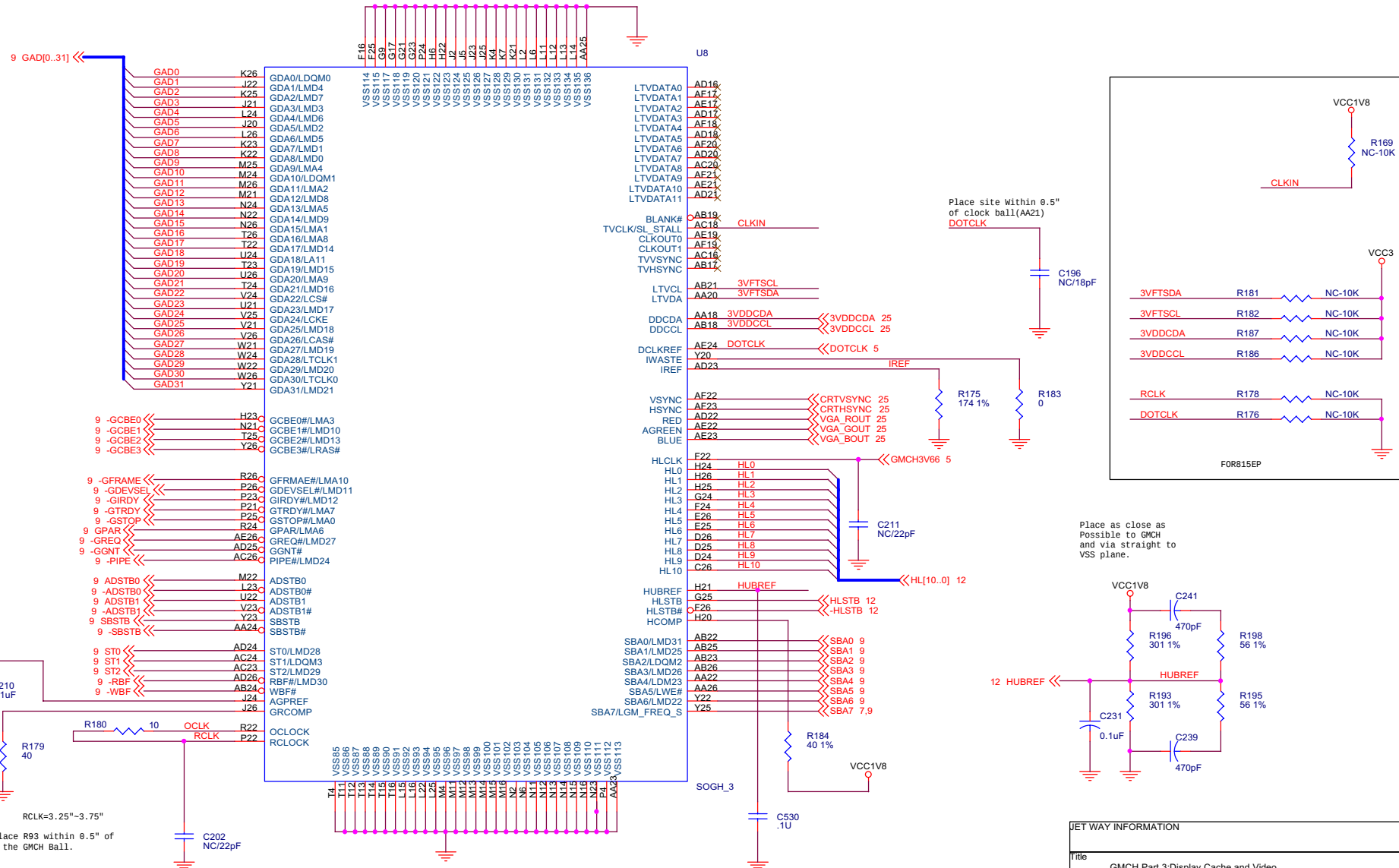




JET WAY INFORMATION			
Title			
GMCH,Part:Host Interference			
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Use surface mount caps
placed close as possible
to power pins with short,
wide direct connections.



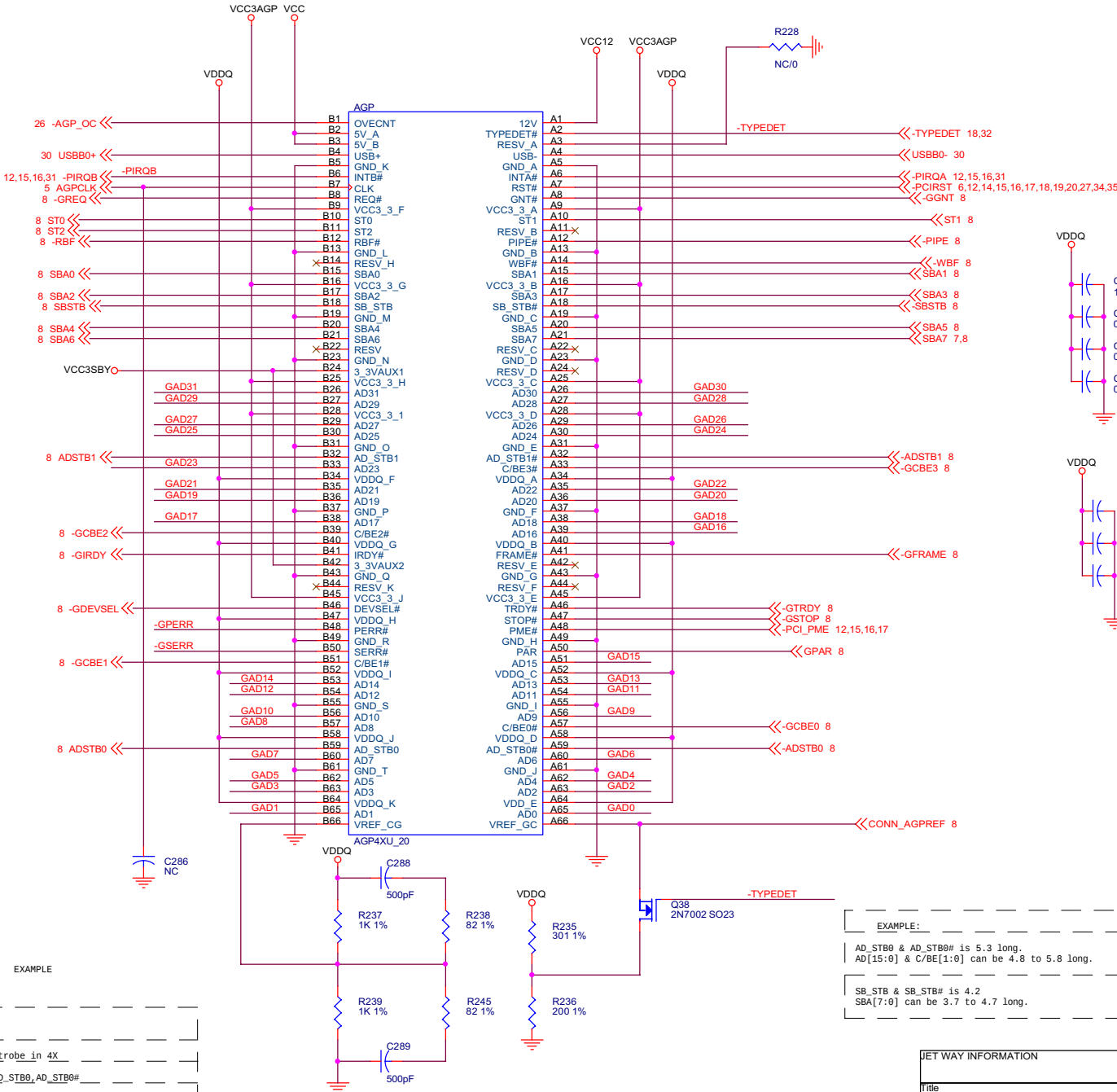
VCC

C275
1uF

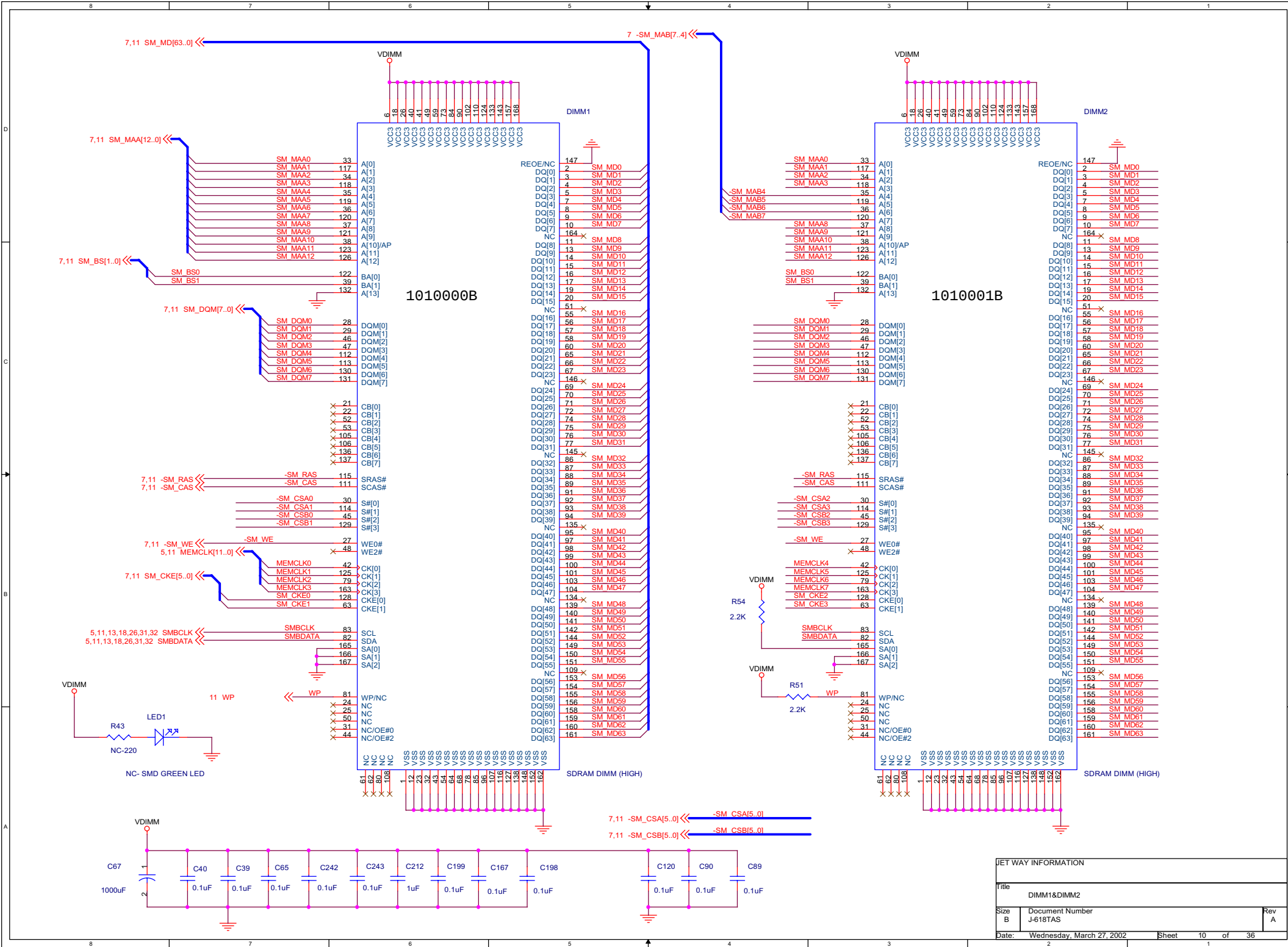
APG_4X



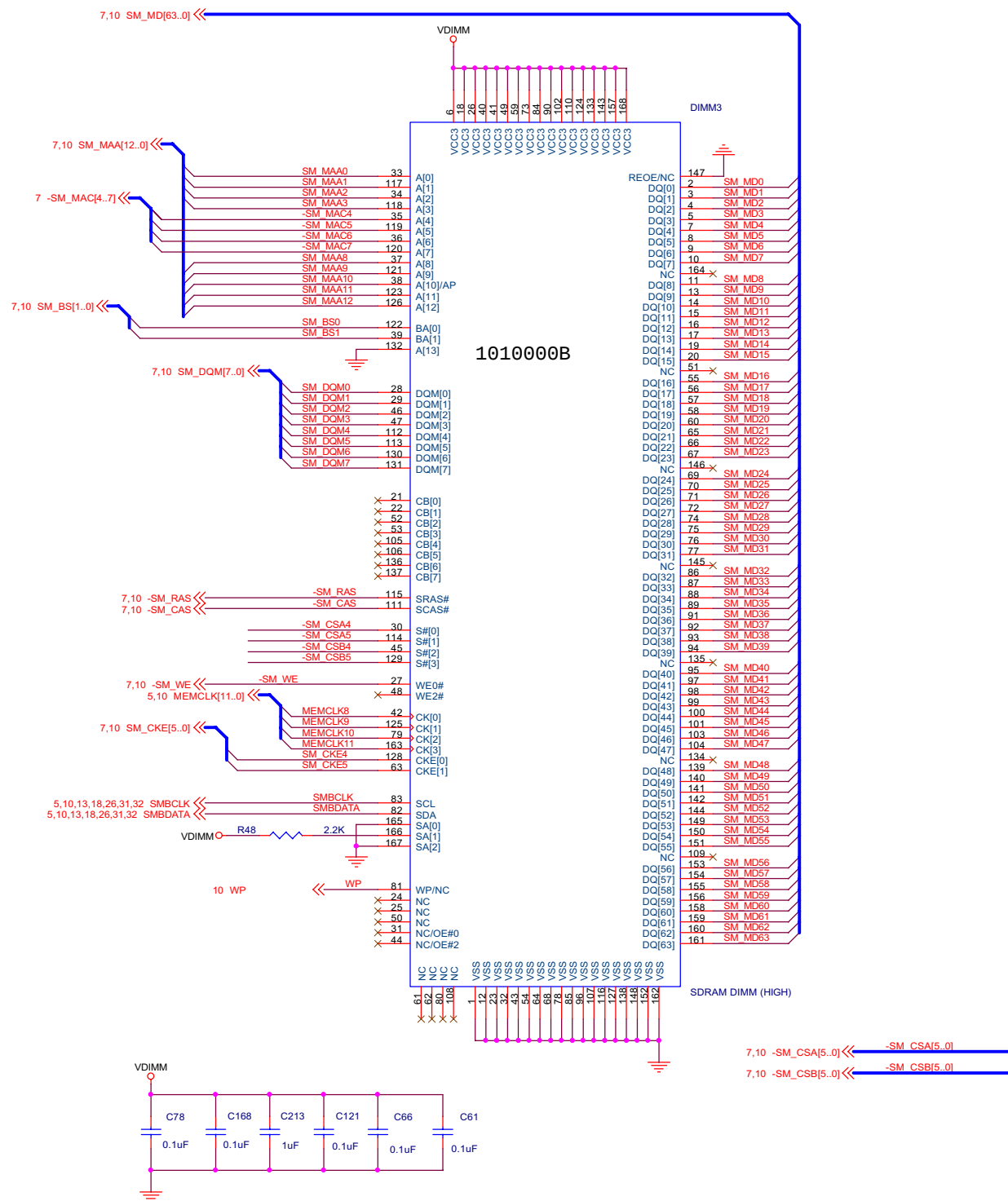
DATA	Strobe in 2X	Strobe in 4X
AD[15:0], C/BE[1:0]#	AD_STB0	AD_STB0, AD_STB#
AD[31:16], C/BE[3:2]#	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	SB_STB	SB_STB, SB_STB#

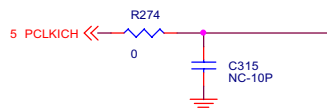
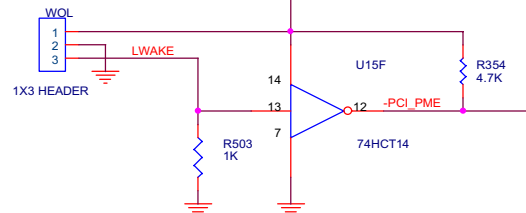
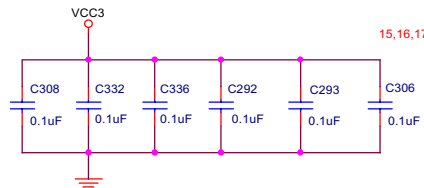


JET WAY INFORMATION			
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AGP SLOT			
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Title			
DIMM1&DIMM2			
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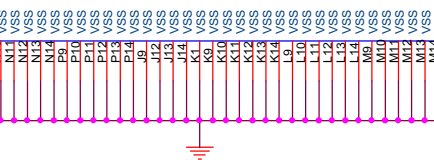


9,15,16,17 -PCI_PME <- -PCI PME

26 LAN_TXD0
26 LAN_TXD1
26 LAN_TXD2
26 LAN_RSTSYNC
26 EE_SHCLK
26 EE_CS
26 EE_DIN
26 EE_DOUT

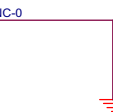
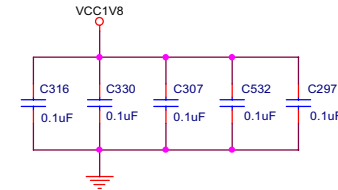
15,16,17,34,35 AD[31..0] <->
15,16,17,34,35 -C_BE[3..0] <->
15,16,17,31,34,35 -FRAME
15,16,17,31,34,35 -DEVSEL
15,16,17,31,34,35 -IRDY
15,16,17,31,34,35 -TRDY
15,16,17,18,31,34,35 -STOP
15,16,17,31 -PLOCK
15,16,17,34,35 PAR
15,16,17,31 -SERR
15,16,17,31 -PERR
31 -PREQA
31 -PGNTA
17,31 -PREQ5
17,31 -PGNT5
26 LAN_TXD0
26 LAN_TXD1
26 LAN_TXD2
26 LAN_RSTSYNC
26 EE_SHCLK
26 EE_CS
26 EE_DIN
26 EE_DOUT

C_BE#0
C_BE#1
C_BE#2
C_BE#3
PCICLK
FRAME#
DEVSEL#
IRDY#
TRDY#
STOP#
PCIRST#
PLOCK#
PAR
SERR#
PERR#
PME#
REQ#/GPIO0
GNT#/GPIO16
REQ#/BREQ5/GPIO1
GNTB#/GPIO17
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_RSTSYNC
EE_SHCLK
EE_CS
EE_DIN
EE_DOUT

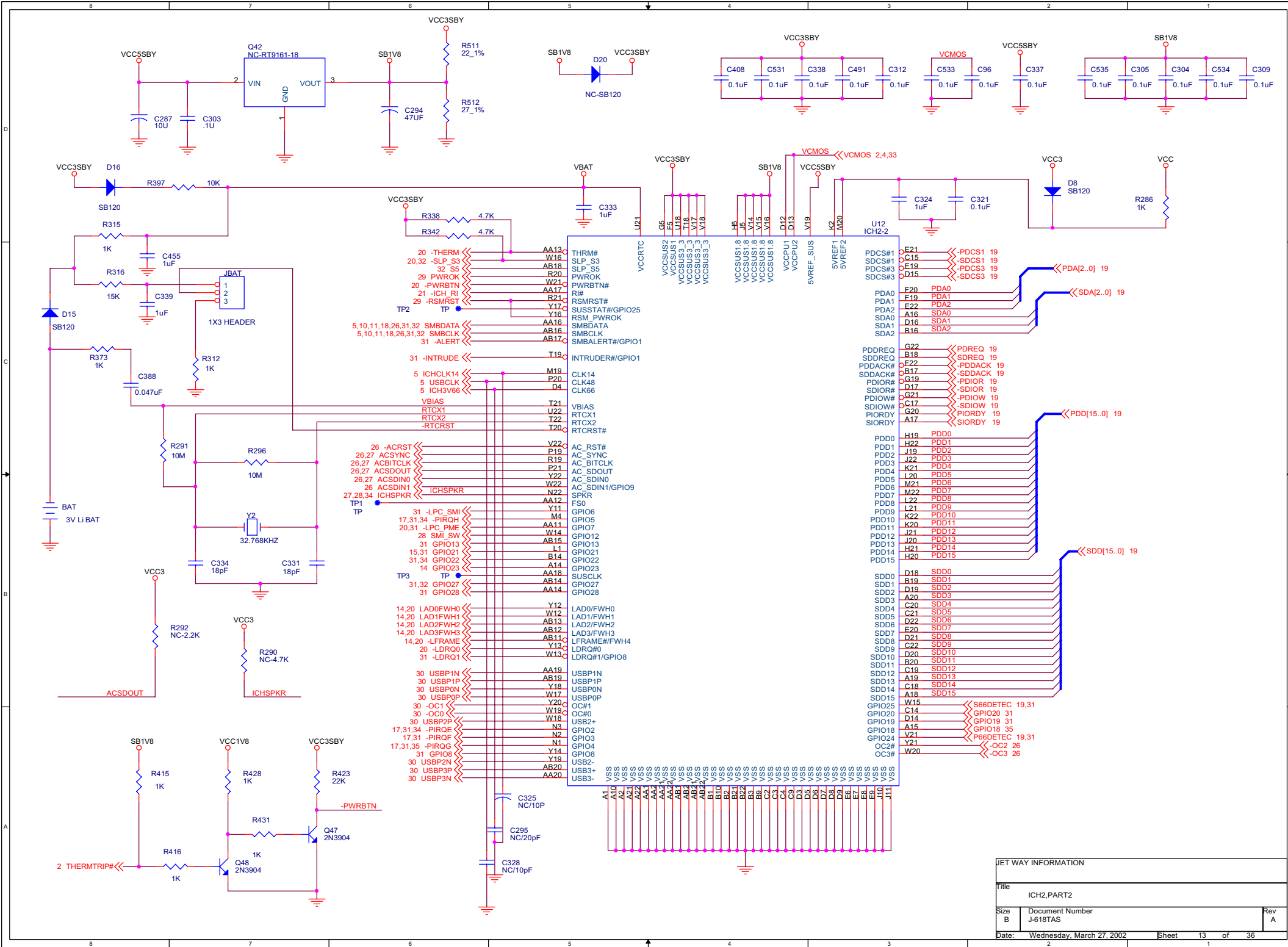


PWRGOOD
A20M#
CPUSLPS#
FERR#
IGNNE#
INTR#
NMI#
SMI#
STPCLK#
RCIN#
A20GATE
HL0
HL1
HL2
HL3
HL4
HL5
HL6
HL7
HL8
HL9
HL10
HLSTB
HLSTB#
HCOMP
HUBREF
VRM-PWRGD
PIRQA#
PIRQB#
PIRQC#
PIRQD#
IRQ14
IRQ15
APICCLK
APICD1
APICD0
SERIRQ
REQ#0
REQ#1
REQ#2
REQ#3
GNT#0
GNT#1
GNT#2
GNT#3
GNT#4
REQ#4
HL11
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_CLK
SMLINK0
SMLINK1

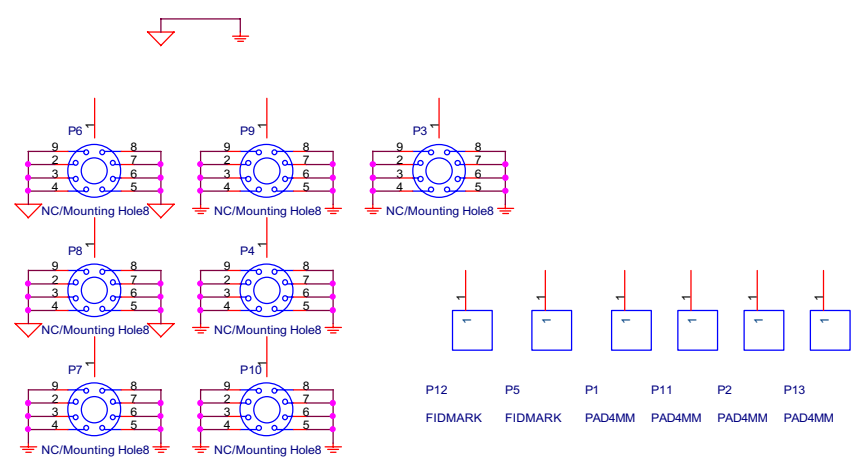
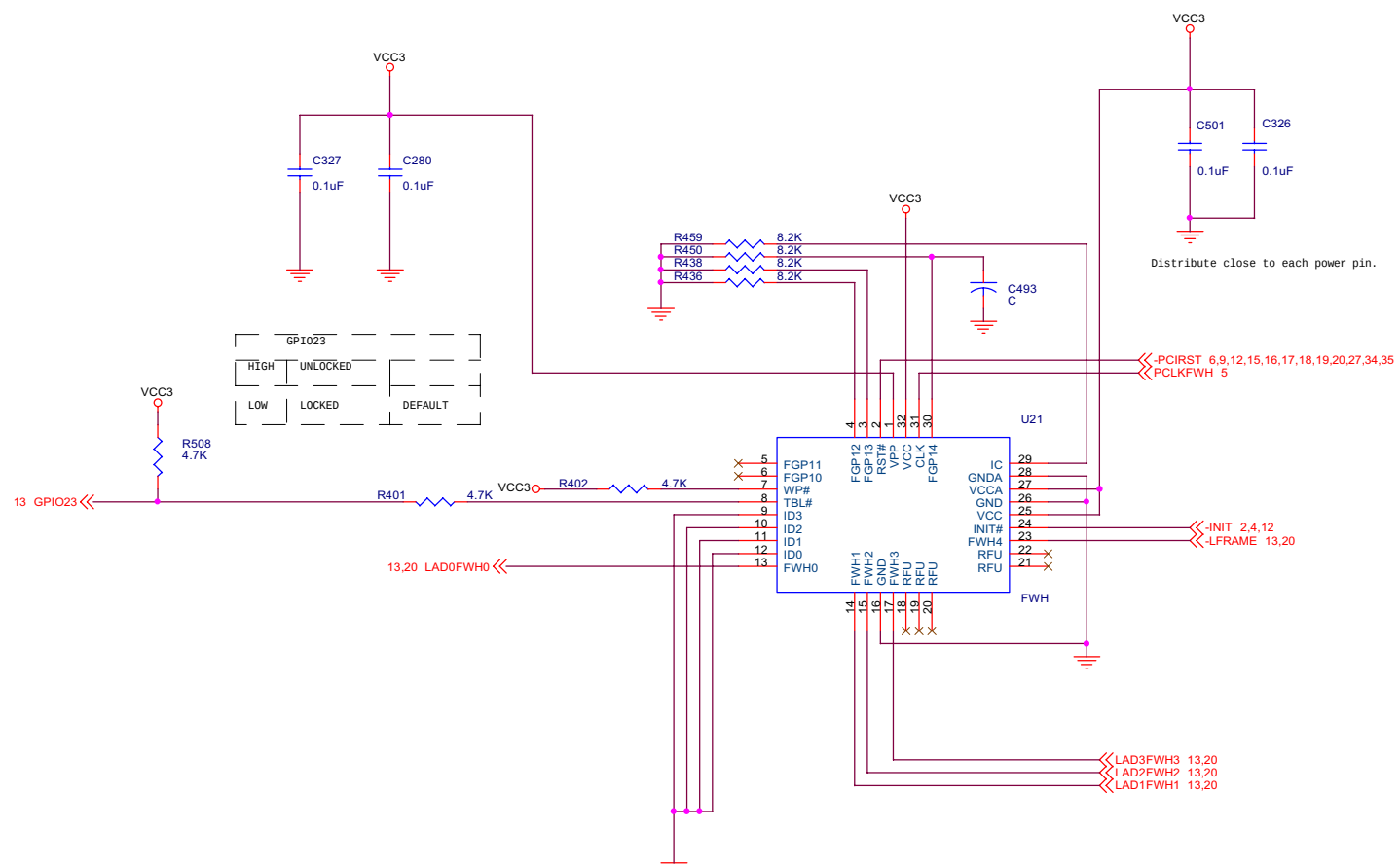
PWRGOOD 2,29
A20M 2
-CPUSLP 2
-FERR 2,4
-IGNNE 2,4
-INIT 2,4,14
-INTR 2
-NMI 2
-SMI 2,4
-STPCLK 2,4
-RCIN 20,31
A20GATE 20,31
HL[0..10] 8
HLSTB 8
HLSTB# 8
VRMPWRGD 5,29,32
-PIROA 9,15,16,31
-PIROB 9,15,16,31
-PIROC 15,16,31
-PIROD 15,16,31
IRQ14 19,31
IRQ15 19,31
APICICH 5
APICD1 2,4
APICD0 2,4
SERIRQ 20,31
-PREQ0 15,31
-PREQ1 15,31
-PREQ2 16,31
-PREQ3 18,31
-PGNT0 15,31
-PGNT1 15,31
-PGNT2 16,31
-PGNT3 18,31
-PGNT4 18,31,34
-PREQ4 18,31,34
LAN_RXD0 26
LAN_RXD1 26
LAN_RXD2 26
LAN_CLK 26



JET WAY INFORMATION			
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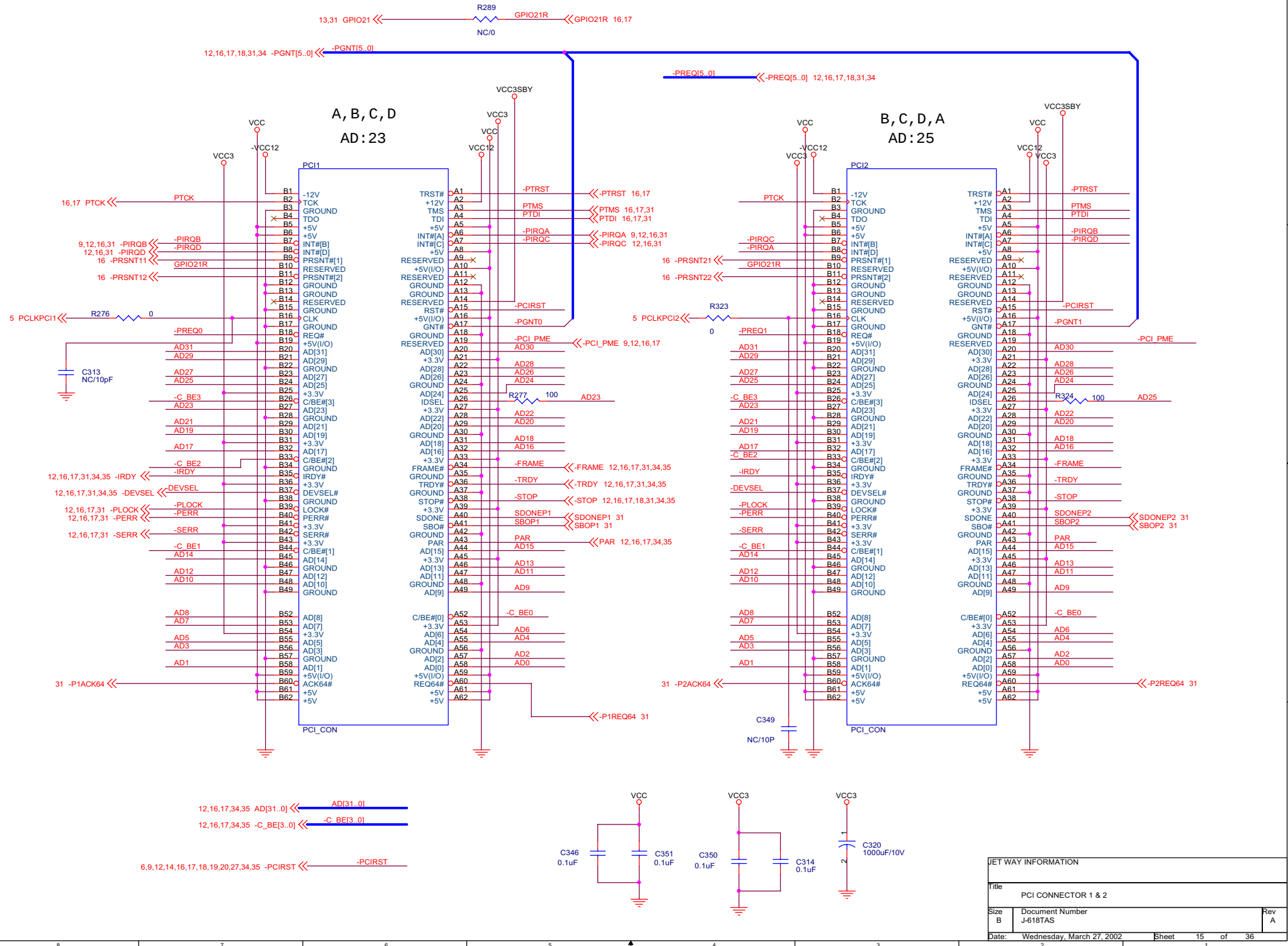
JET WAY INFORMATION		
Title		
ICH2.PART2		
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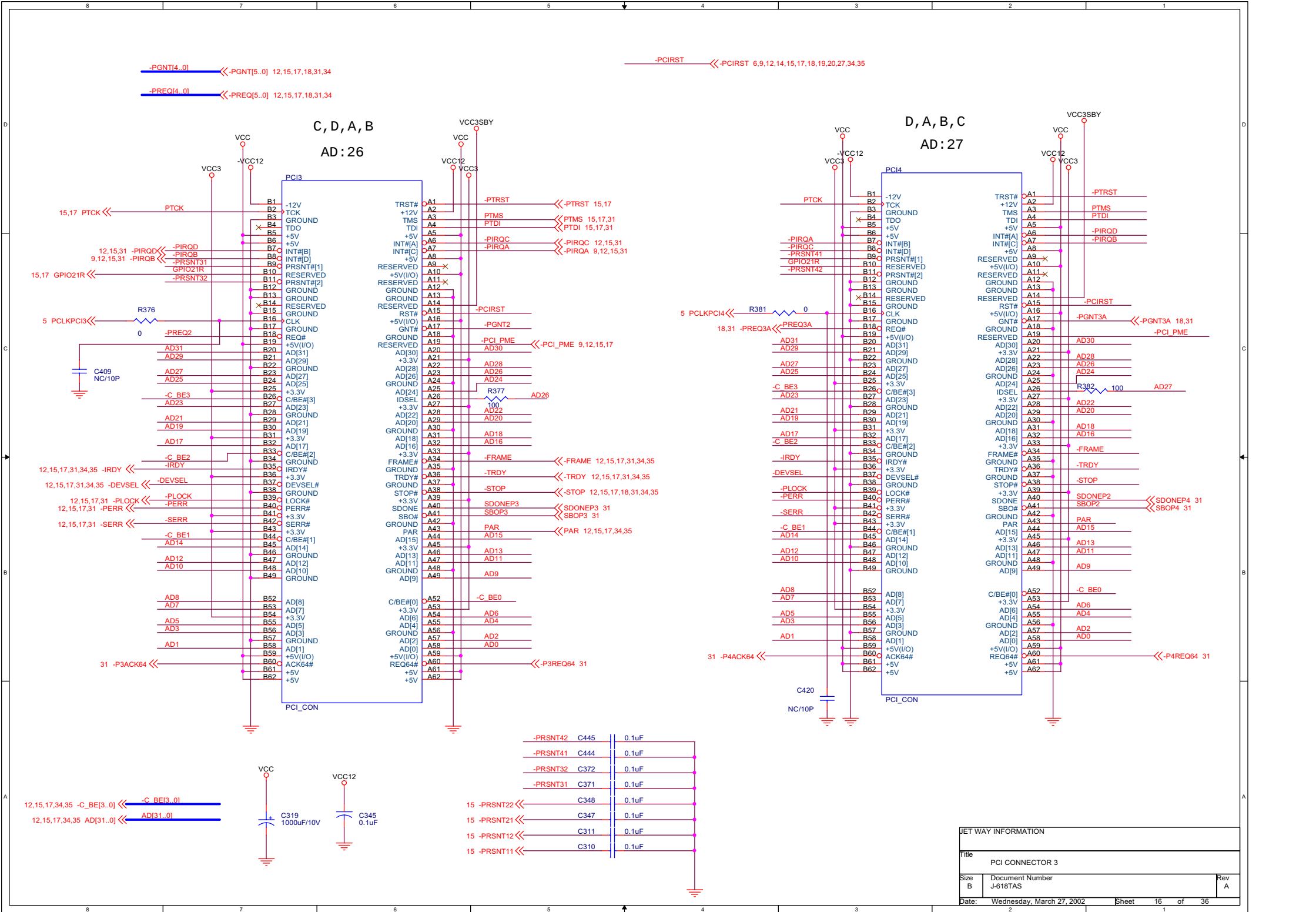
NOTES:

VPP and WP# are tied to VCC3
in this configuration Write Protection is register based
with the exception of the Boot Block.

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FIRMWARE HUB		
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JET WAY INFORMATION		
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PCI CONNECTOR 1 & 2		
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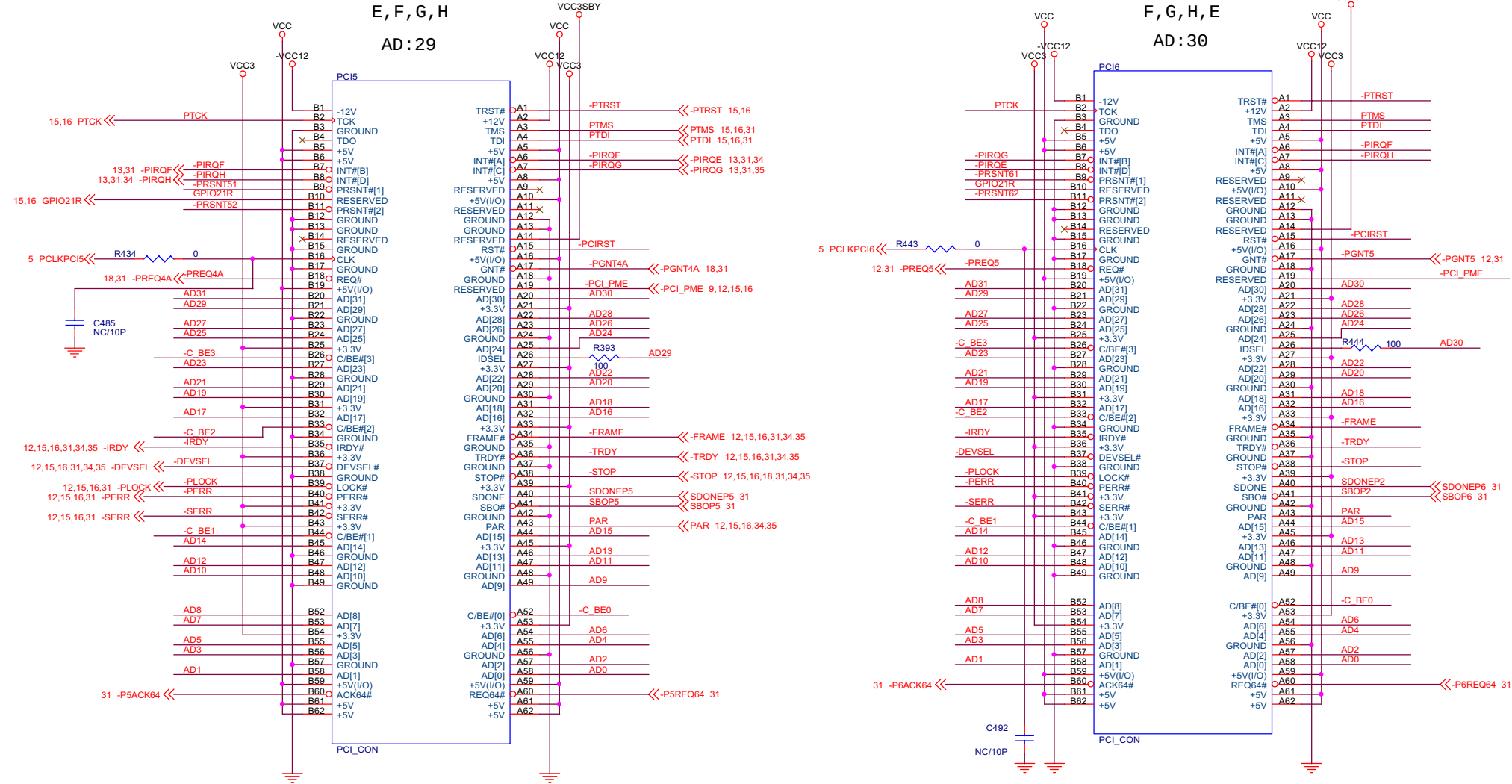


-PGNT[5..0] <<-PGNT[5..0] 12,15,16,18,31,34
-PREQ[5..0] <<-PREQ[5..0] 12,15,16,18,31,34

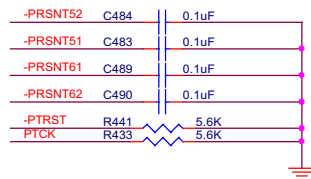
-PCIRST <<-PCIRST 6,9,12,14,15,16,18,19,20,27,34,35

E, F, G, H
AD: 29

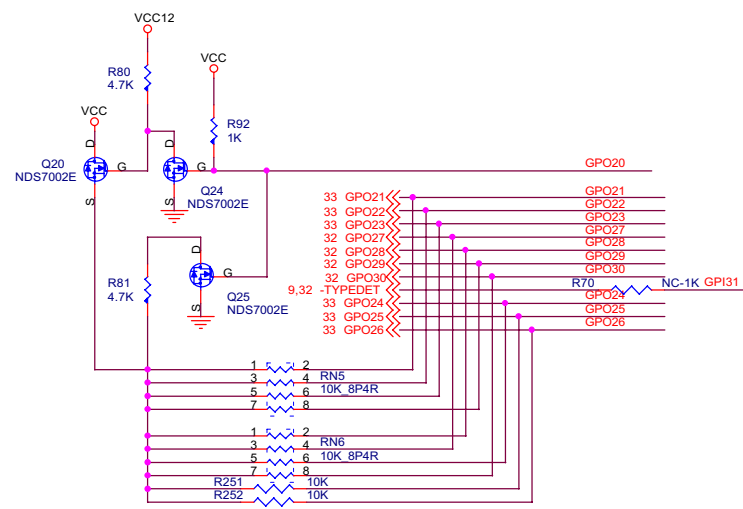
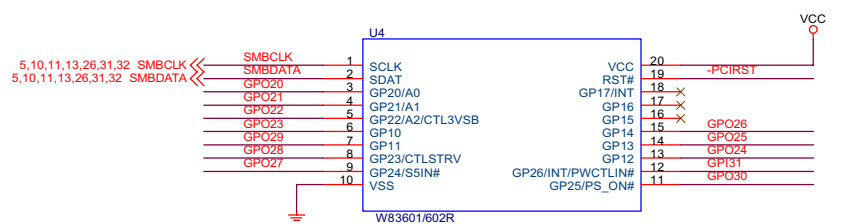
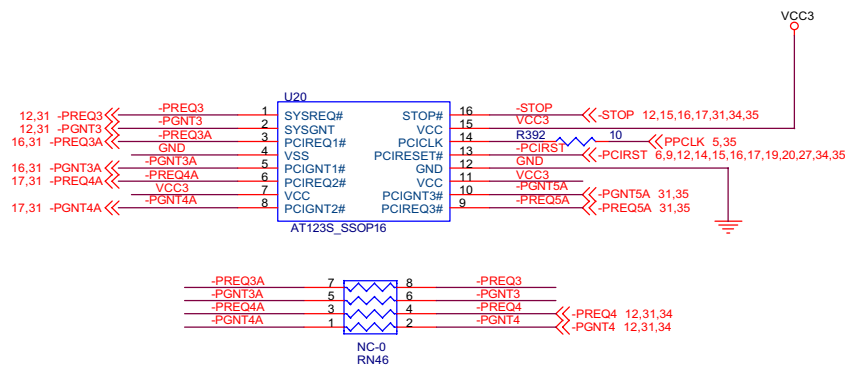
F, G, H, E
AD: 30



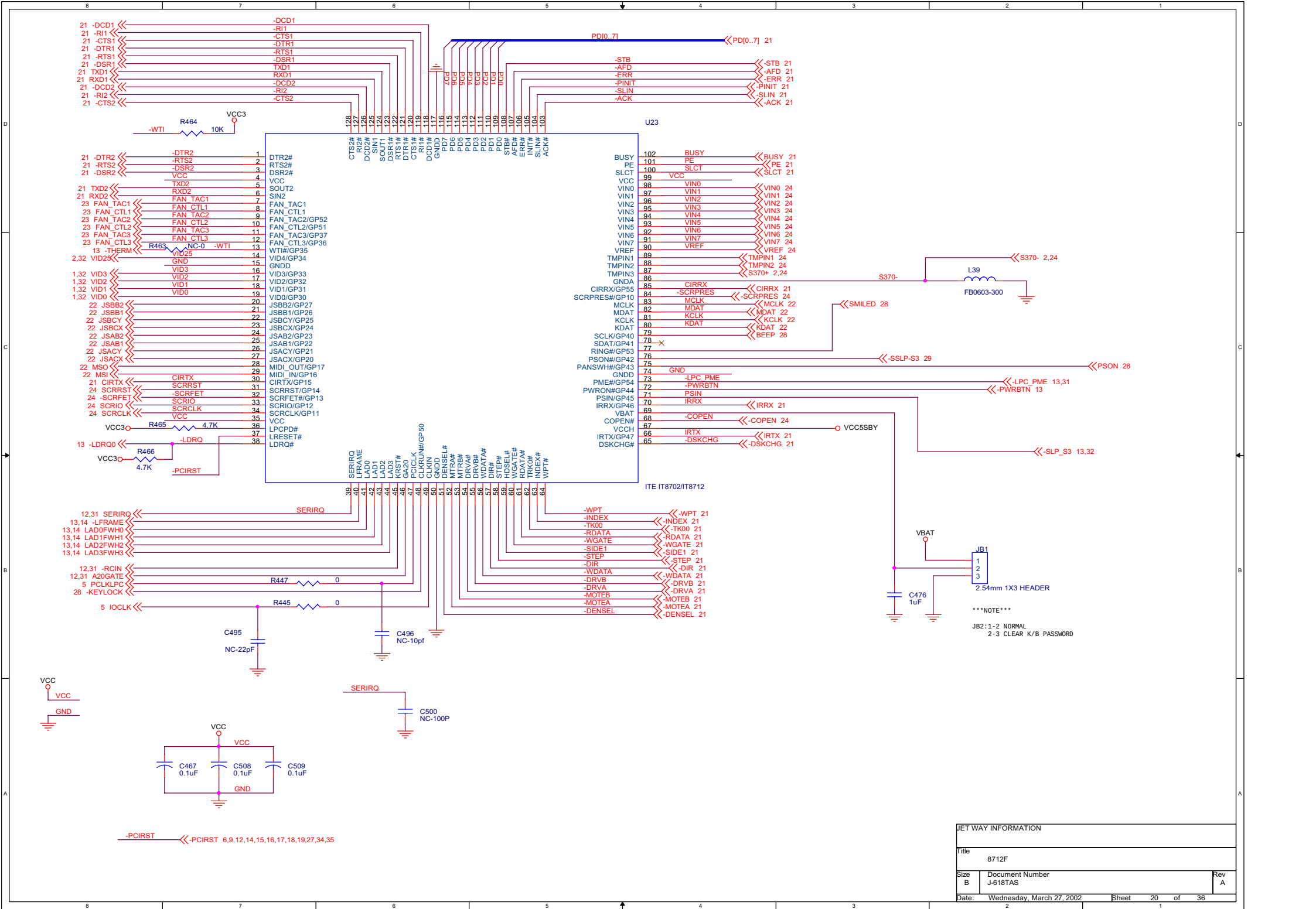
12,15,16,34,35 -C_BE[3..0] <<-C_BE[3..0]
12,15,16,34,35 AD[31..0] <<AD[31..0]

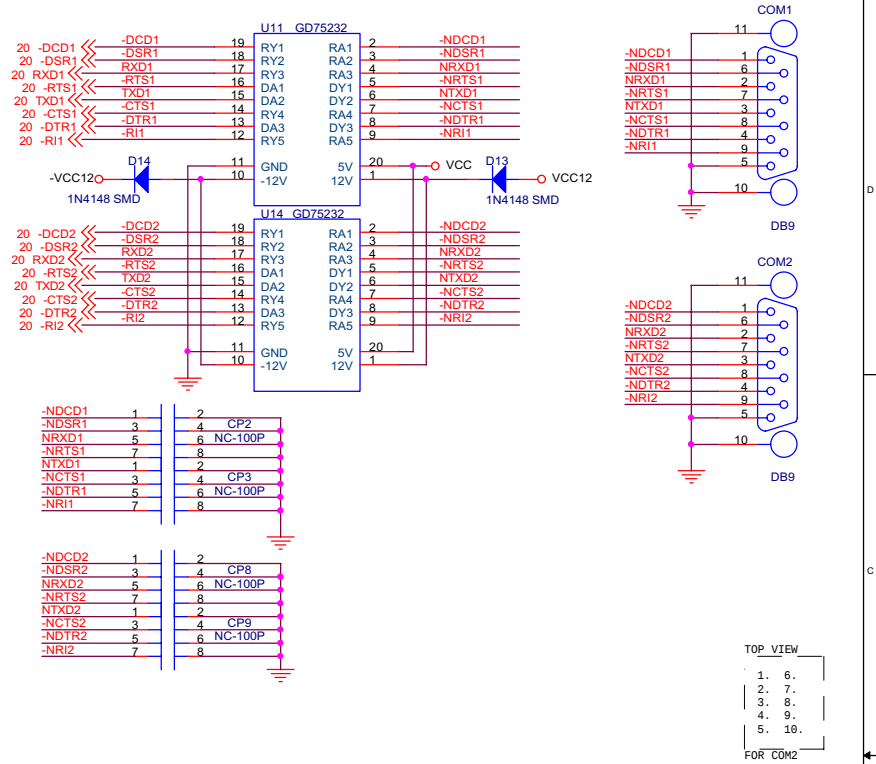
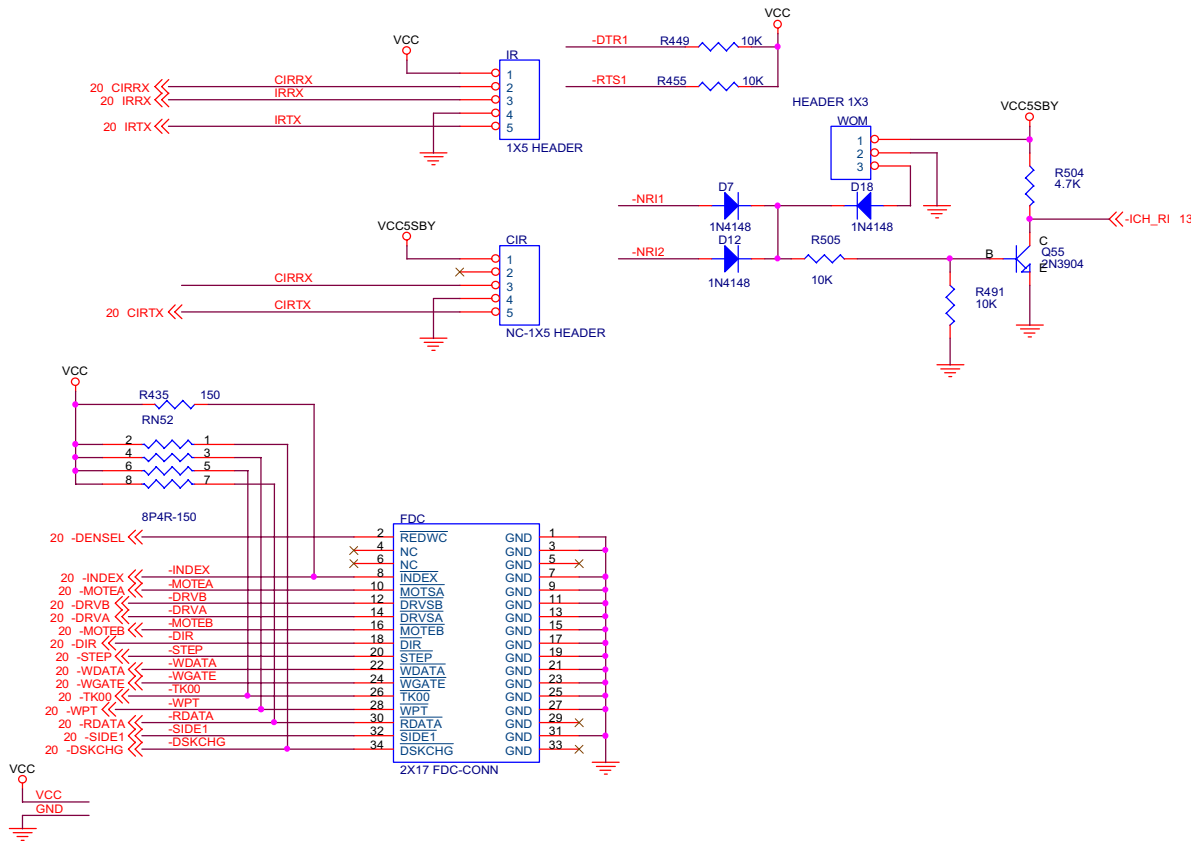


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Title		
PCI CONNECTOR 5&6		
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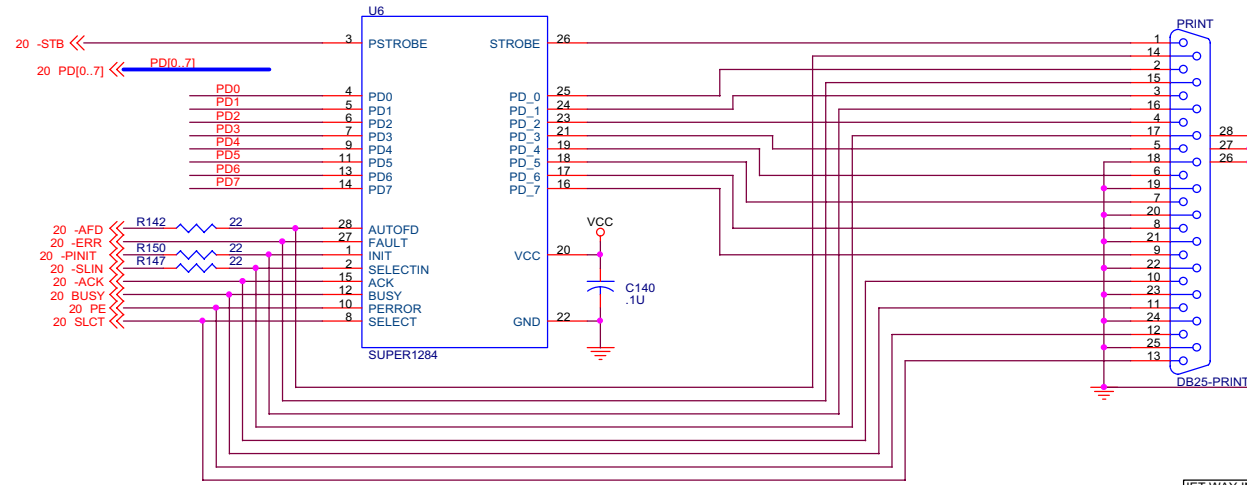


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Title			
GPIO CONTRL&PCI MASTER SELECT			
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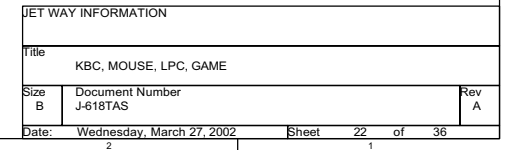
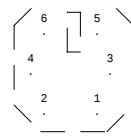


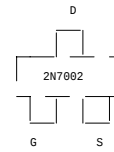
PRT PORT



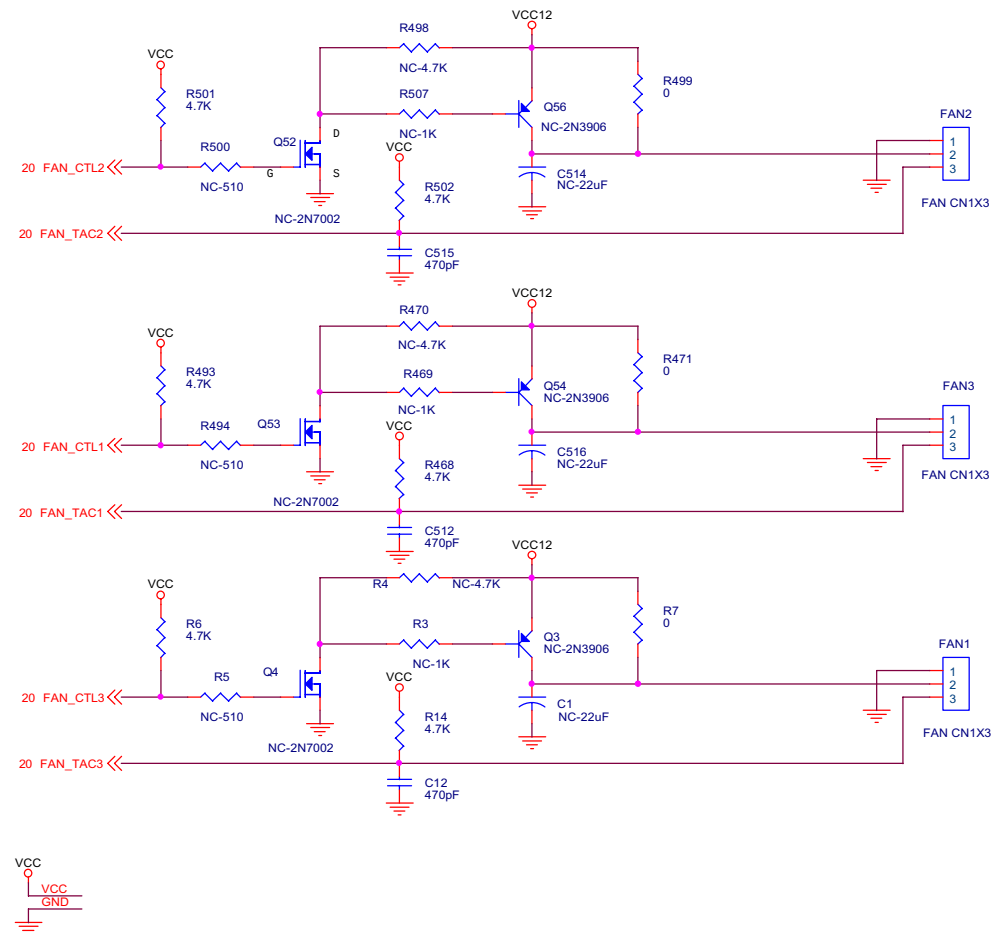
JET WAY INFORMATION			
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I/O CONNECTOR			
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4	2	1	3

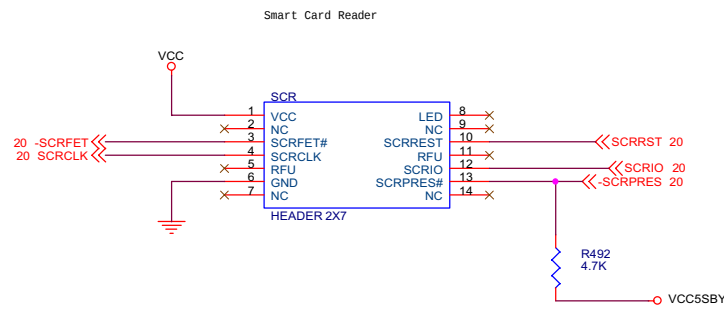
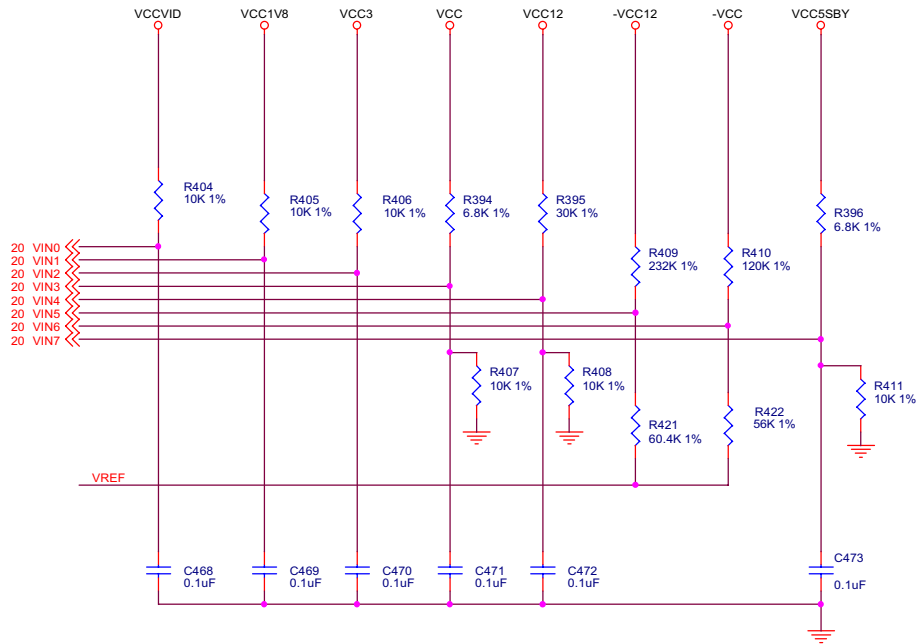
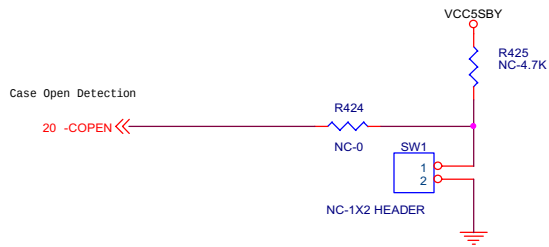
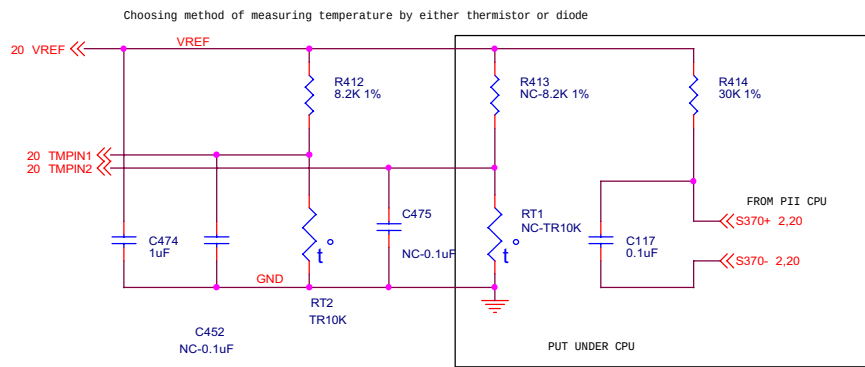


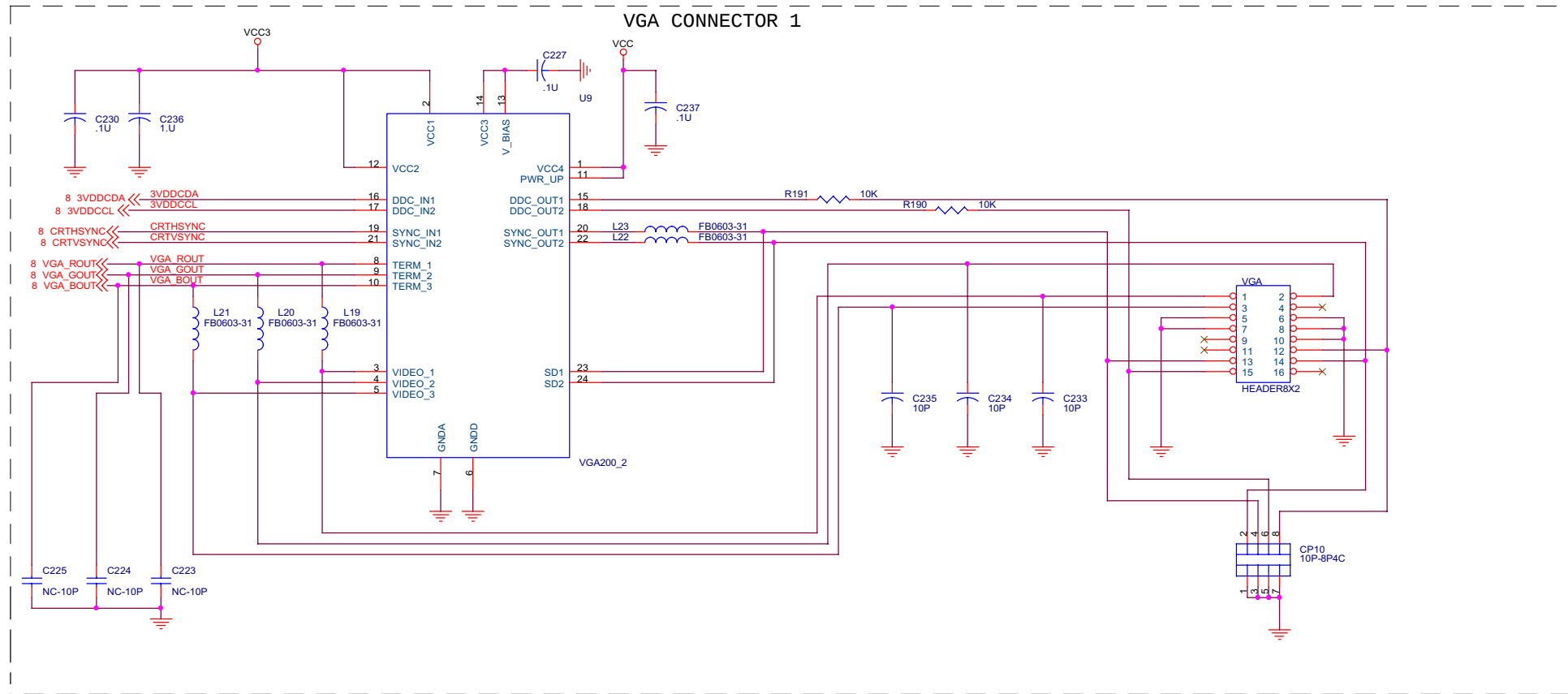


FAN Input and Output

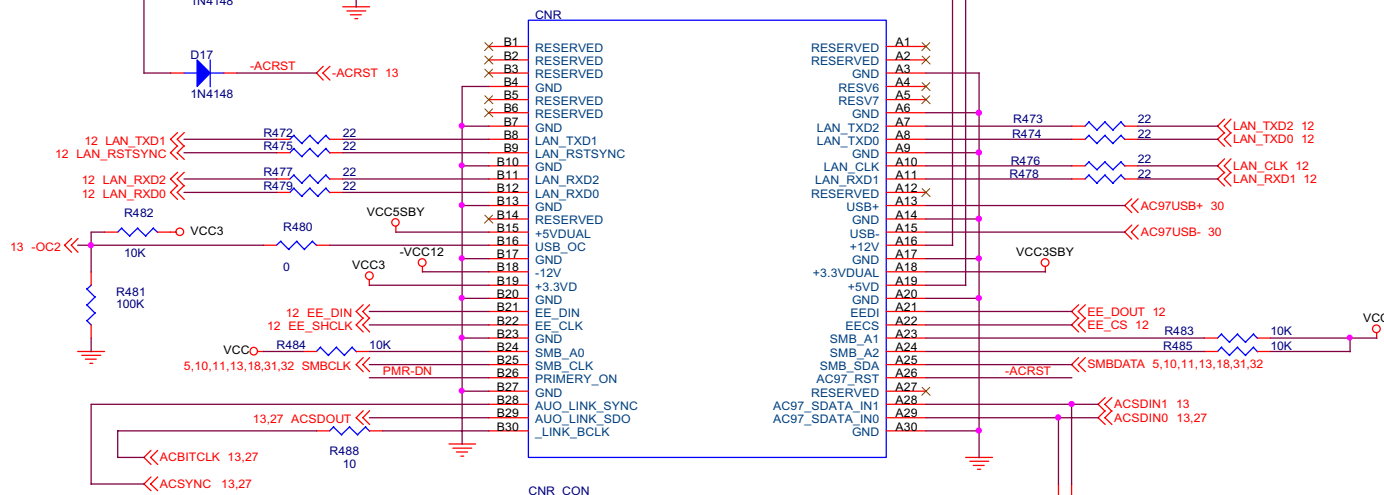
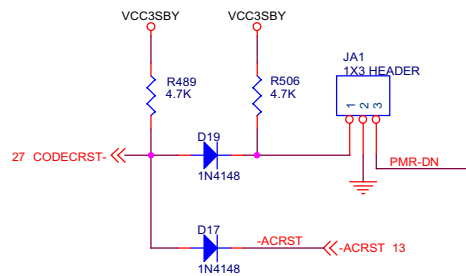
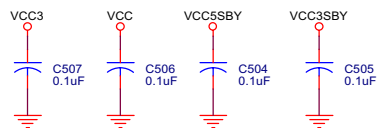
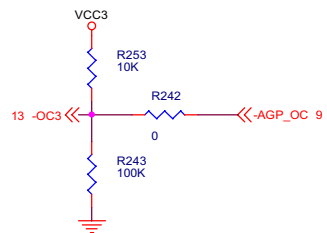


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Game, MIDI Connector			
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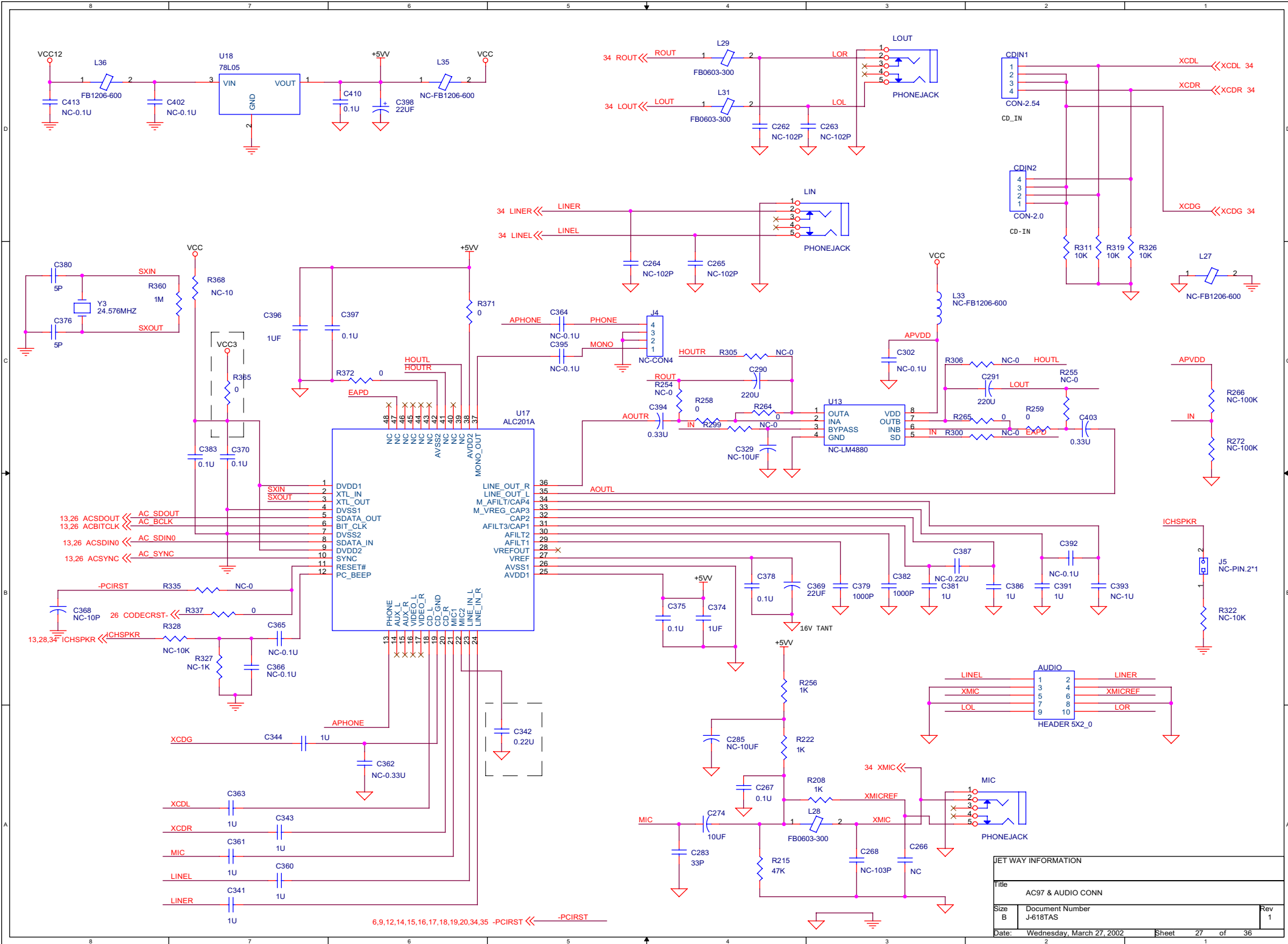


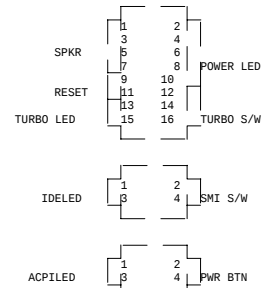
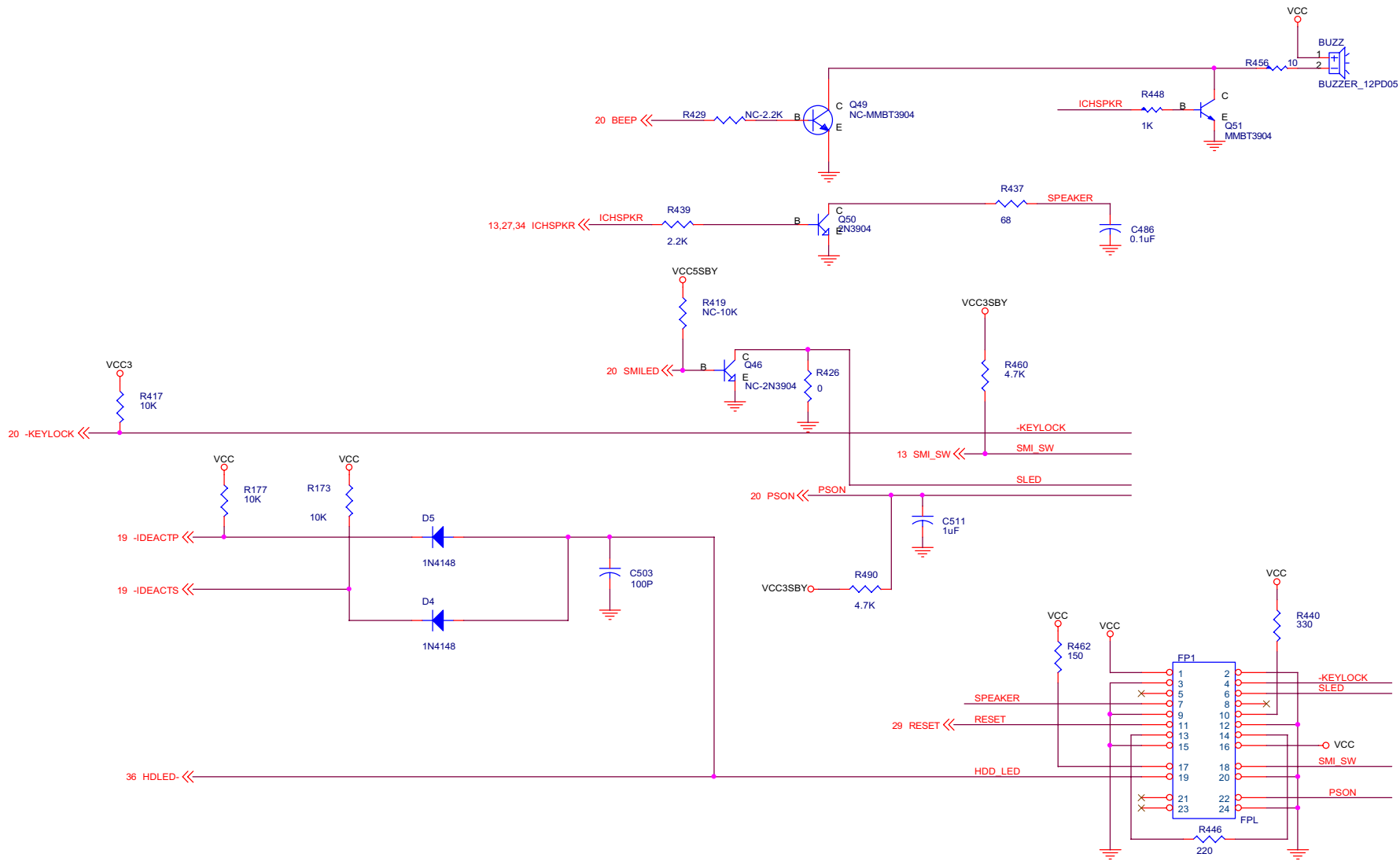


JET WAY INFORMATION			
Title			
VIDEO CONNECTORS			
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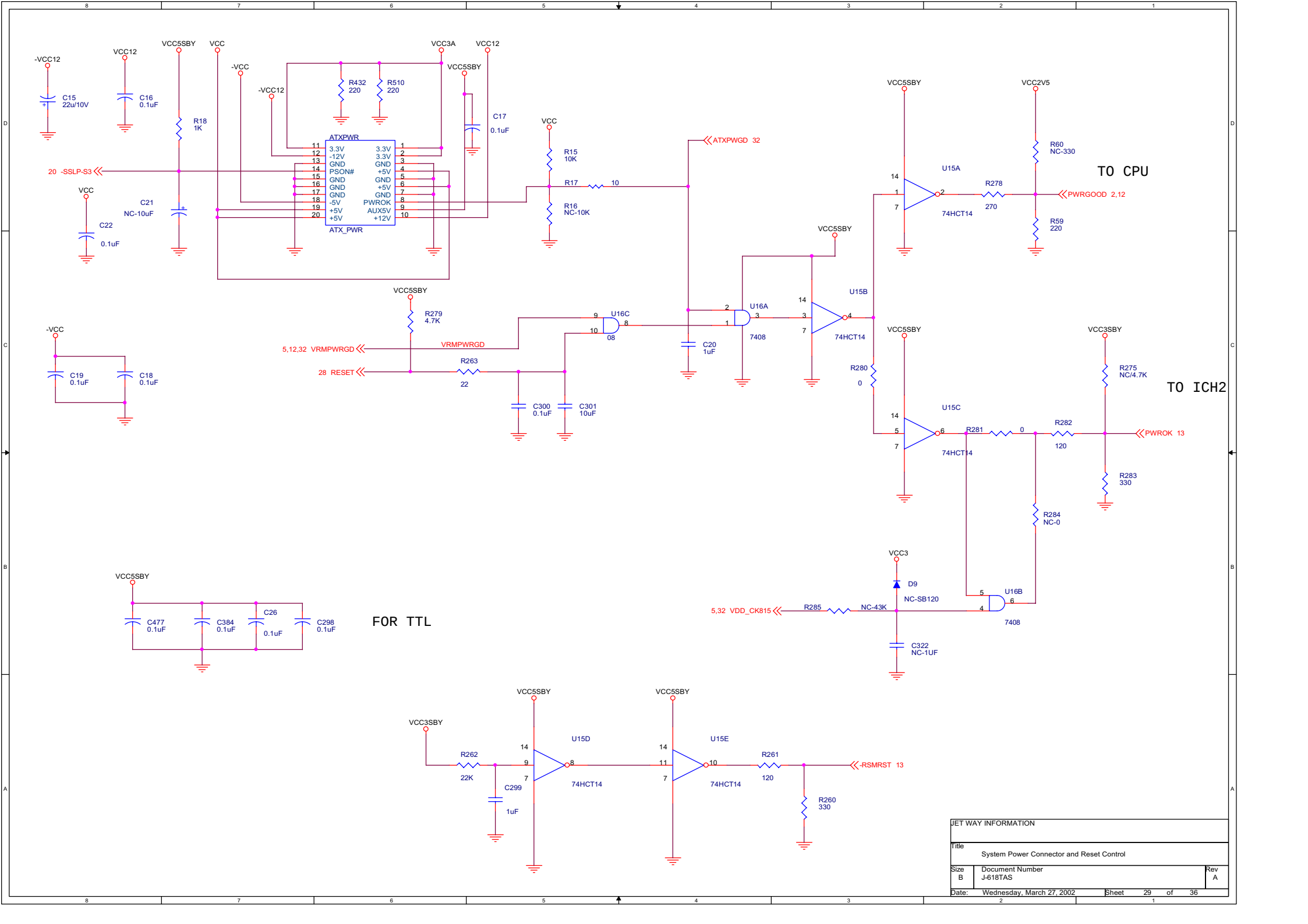


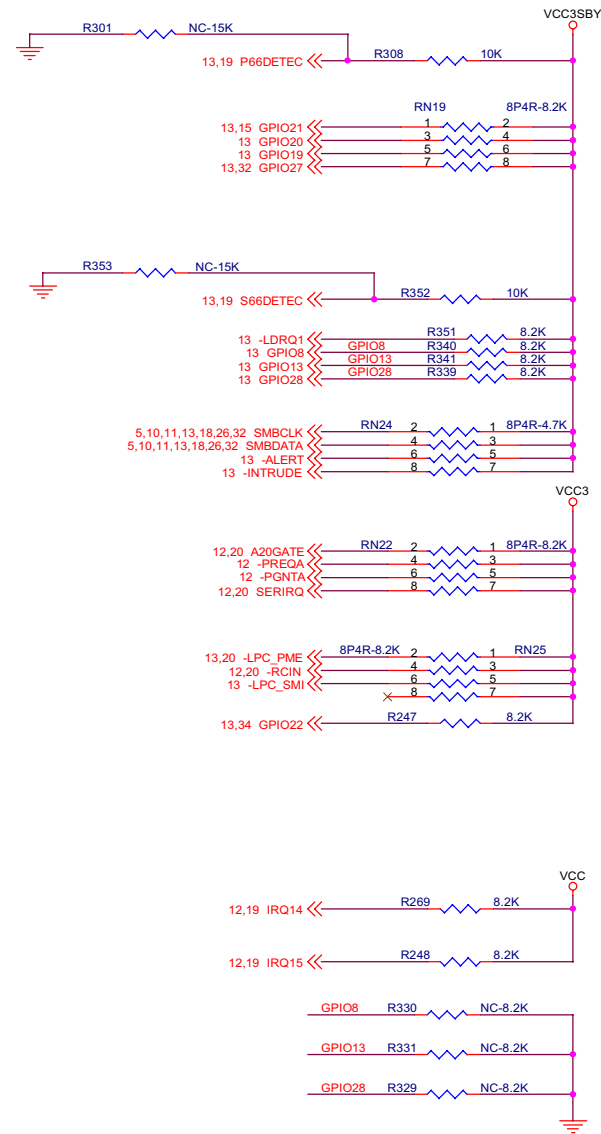
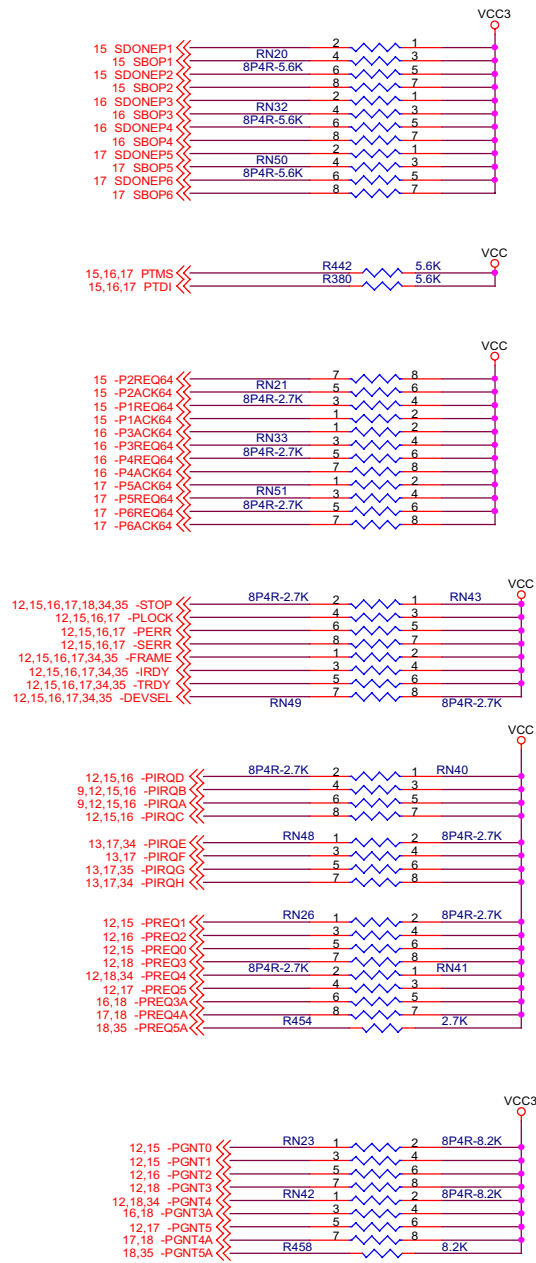
JET WAY INFORMATION			
Title			
CNR CONNECT			
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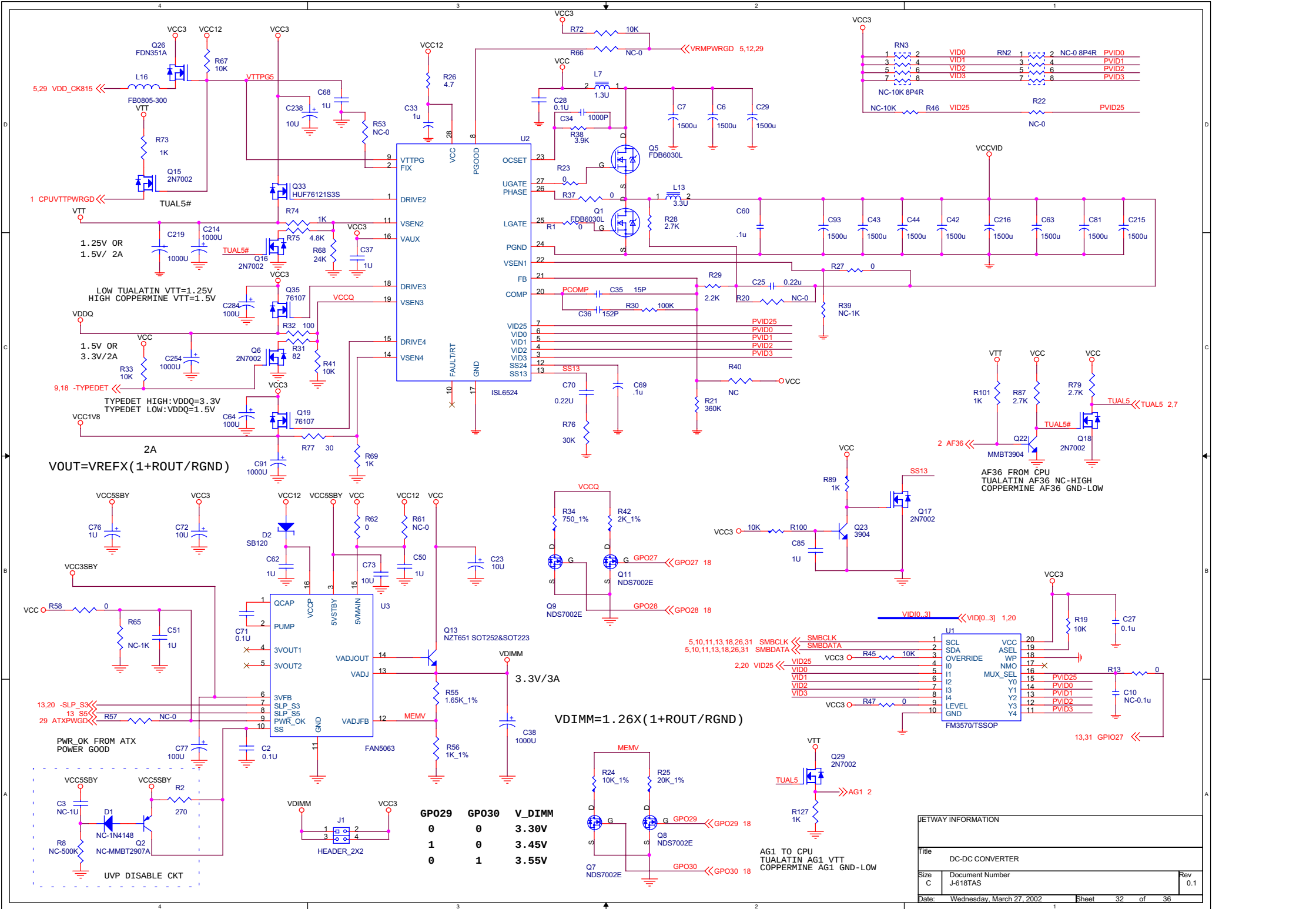


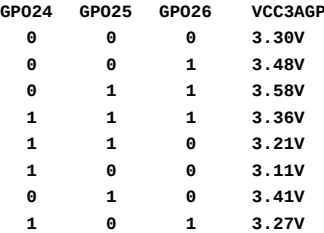
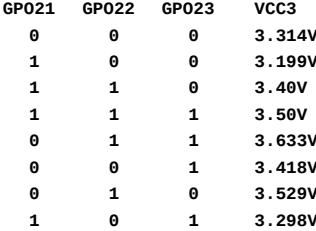
JET WAY INFORMATION		
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SYSTEM		
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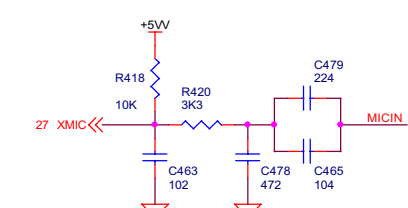
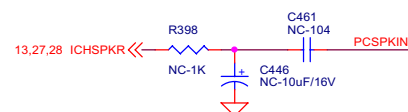
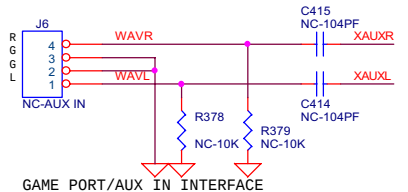
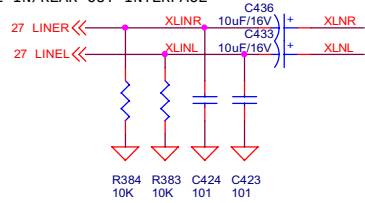
JET WAY INFORMATION			
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PULL-UP RESISTORS			
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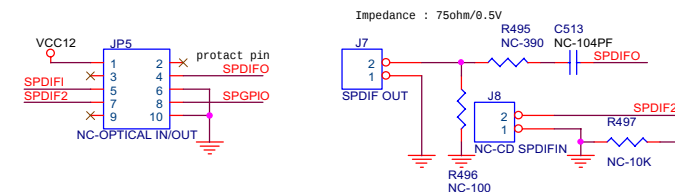


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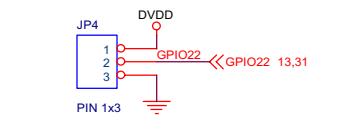
LINE IN/REAR OUT INTERFACE



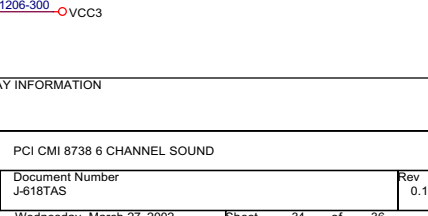
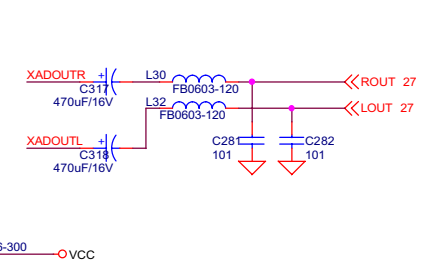
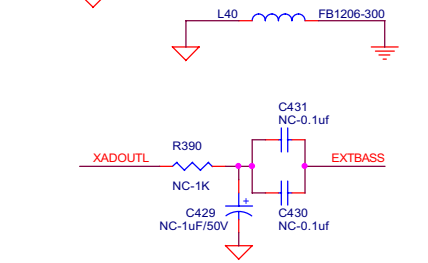
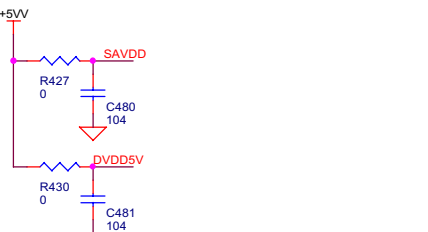
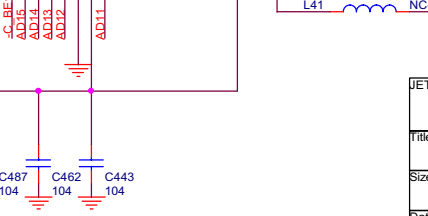
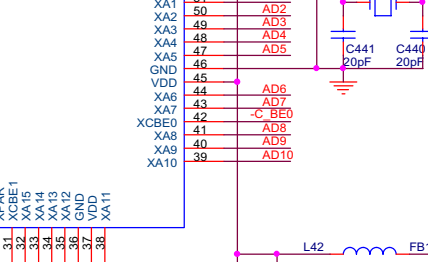
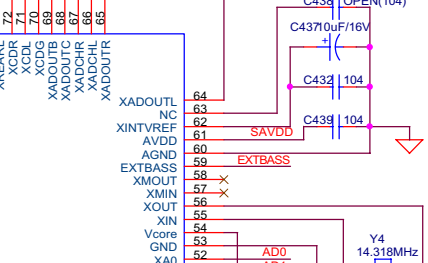
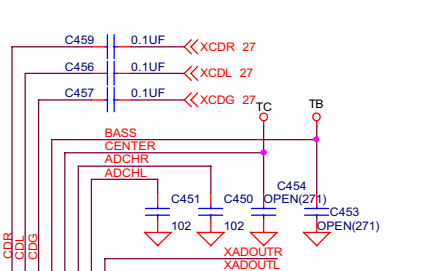
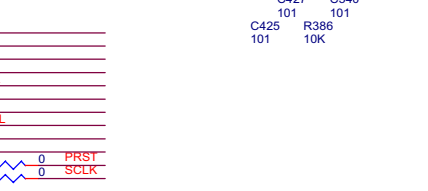
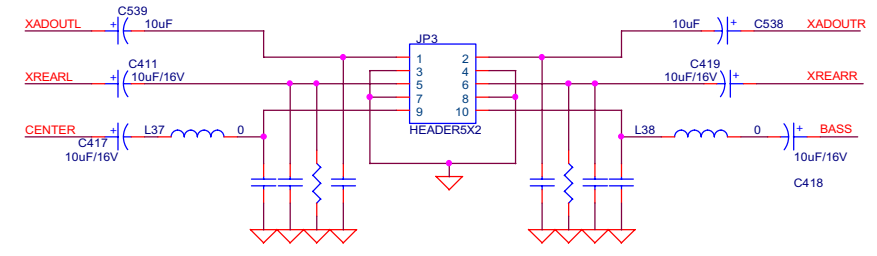
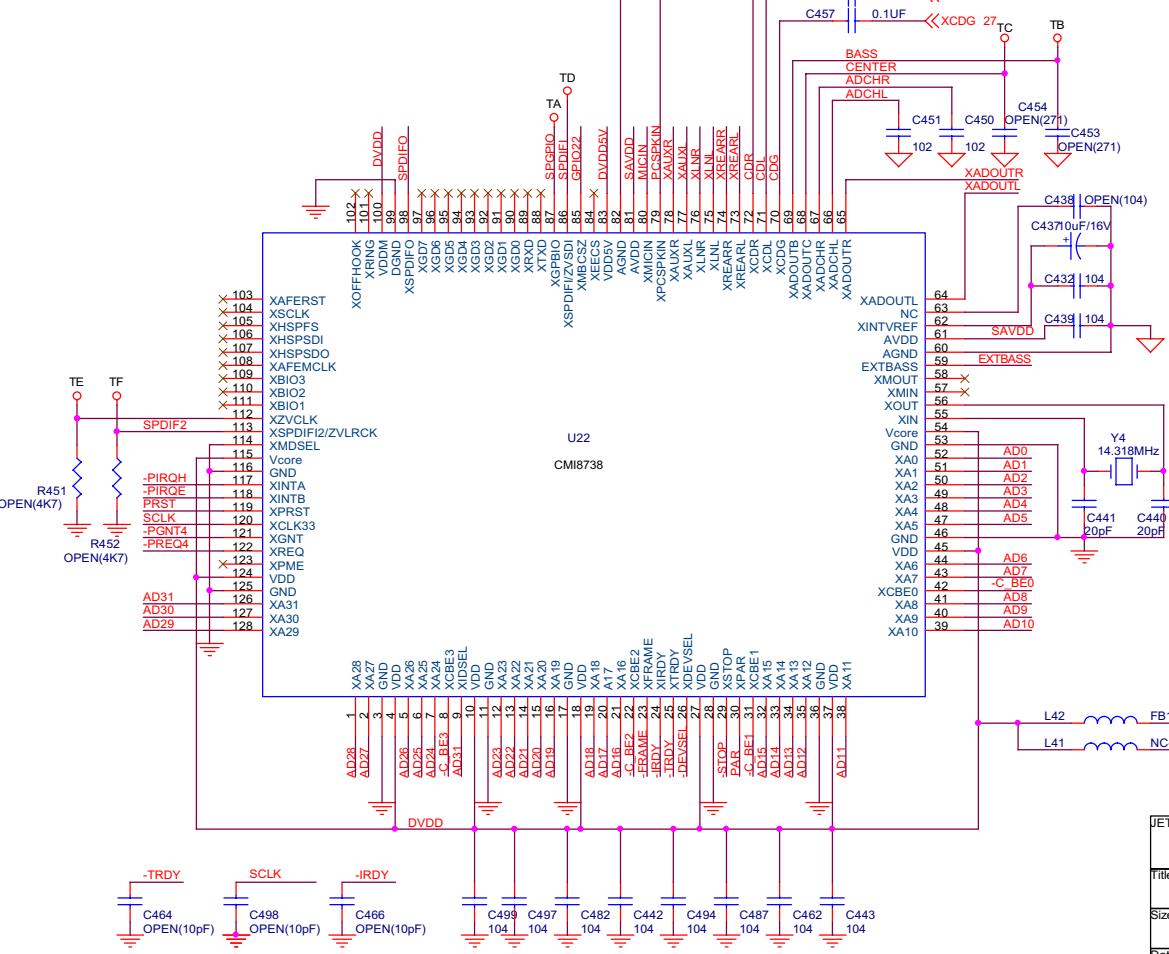
MICROPHONE IN INTERFACE (Option)
** Please see the application note. (APN-M01A)



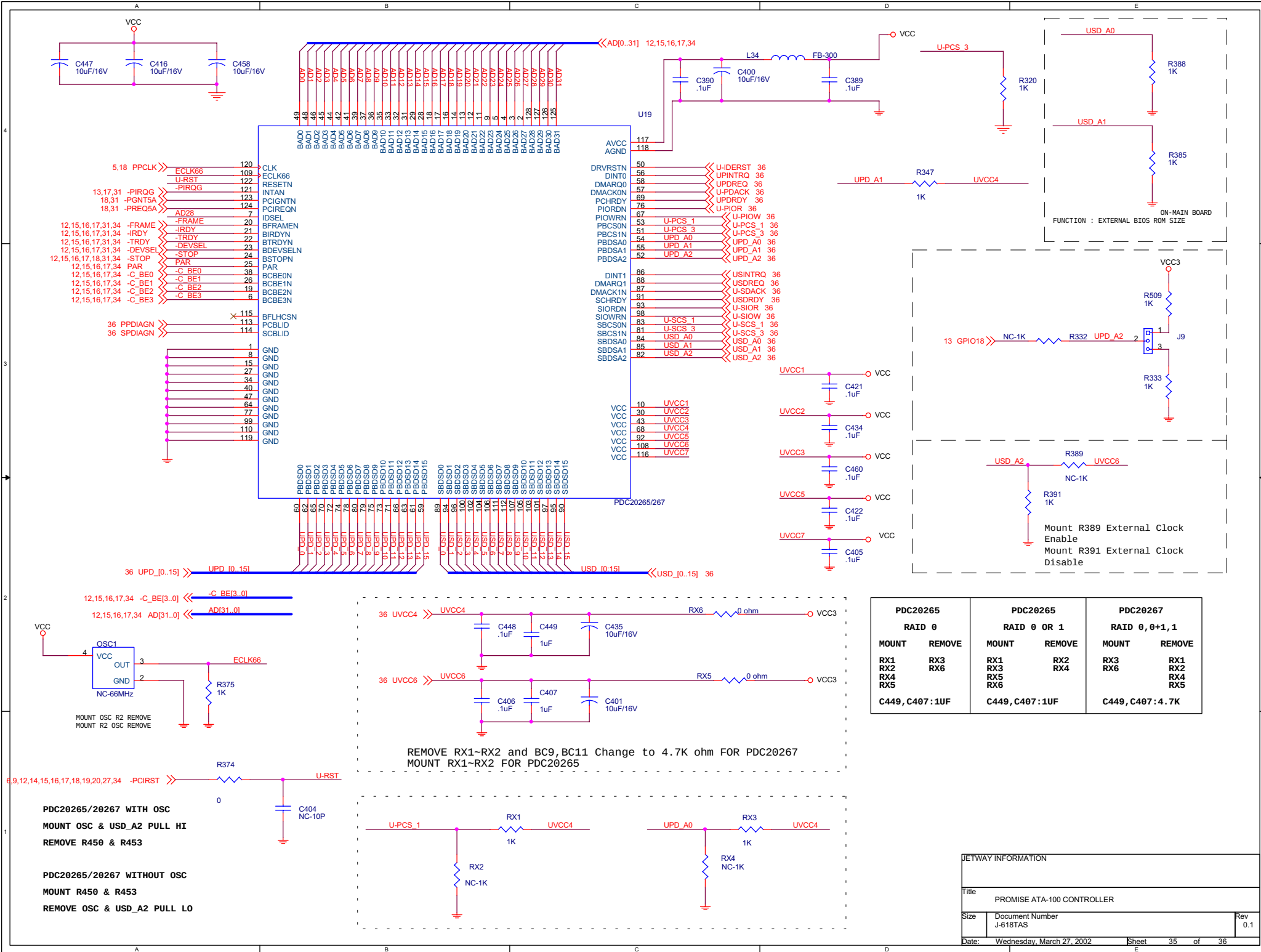
From M/B South Bridge GPIO CONTROL ENABLE
* MBSCT : AUDIO CHIP SELECT
HI : DISABLE
LOW : ENABLE

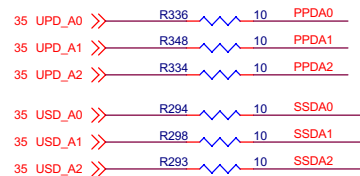
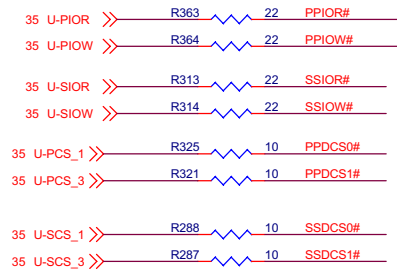
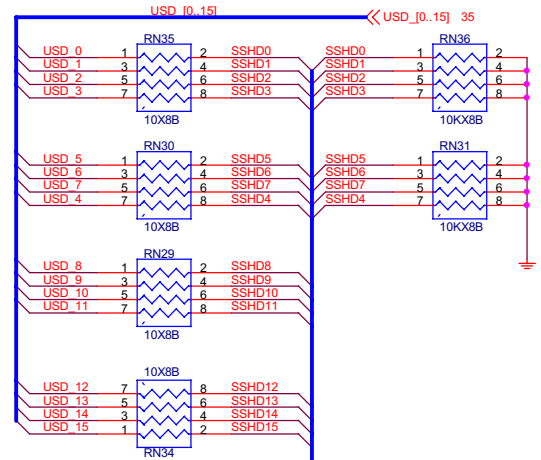
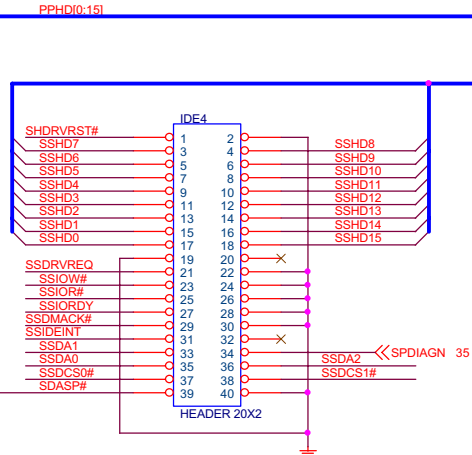
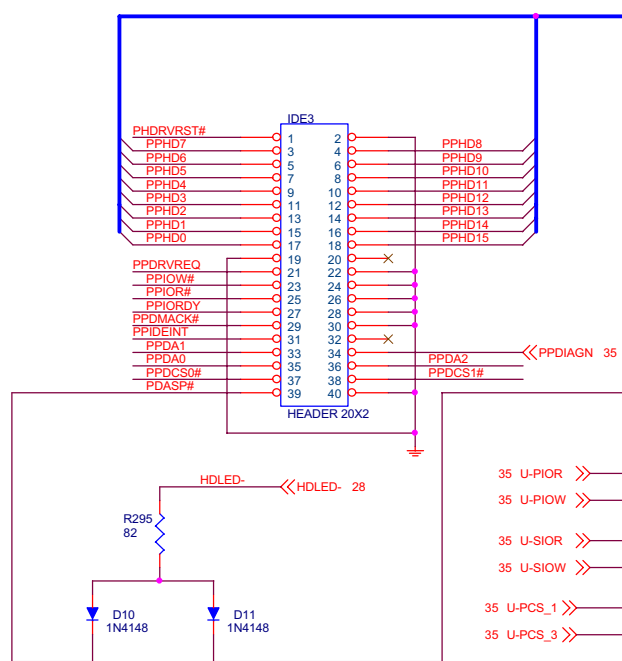
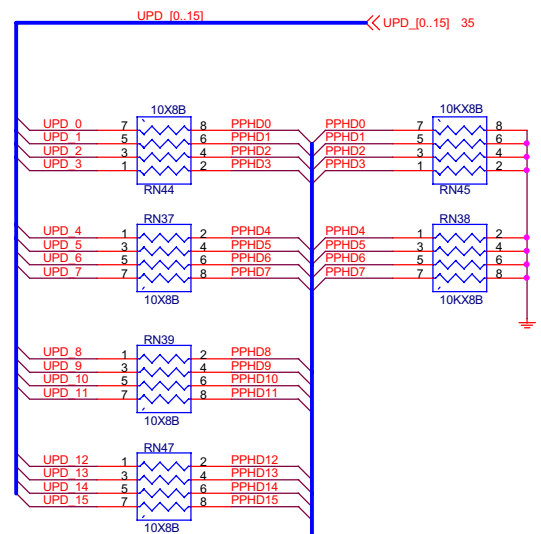
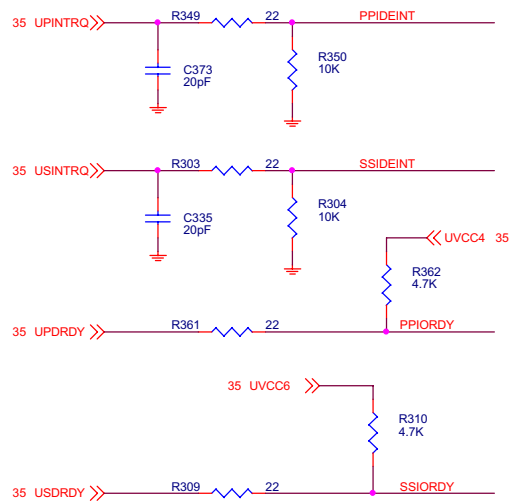
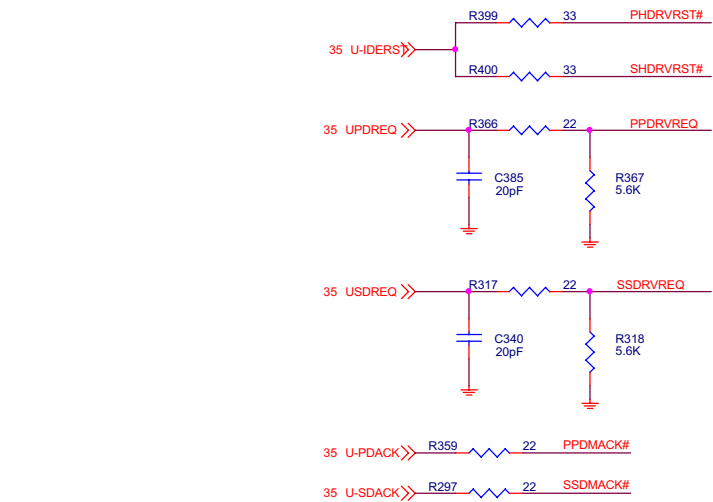


12,15,16,17,35 -C_BE[3..0] <-C_BE[3..0]
12,15,16,17,35 AD[31..0] <-AD[31..0]



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