

JET WAY INFORMATION

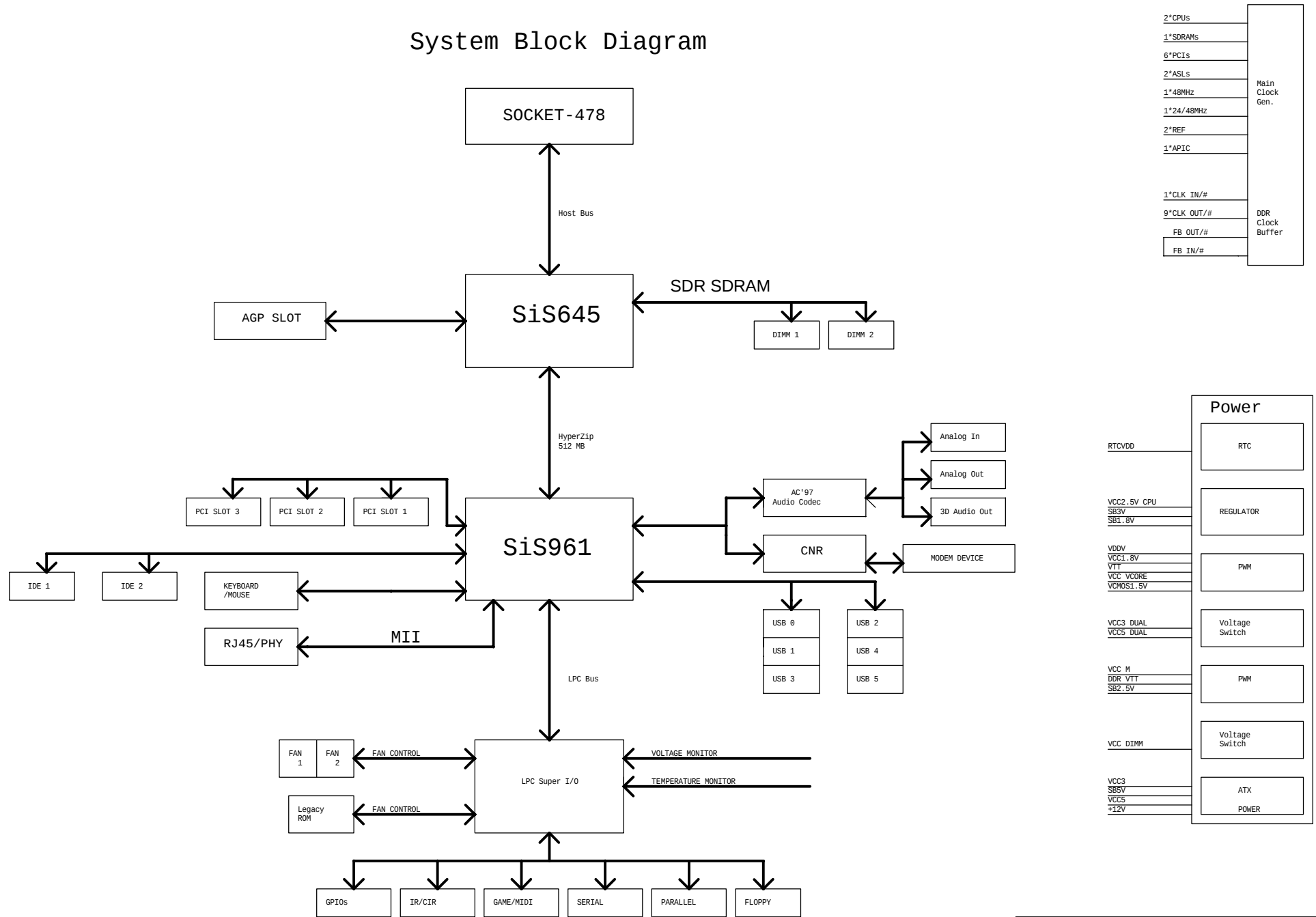
645EM

SiS-645/650 for Pentium 4 (Desktop PC)
Uniprocessor Reference Design Schematics

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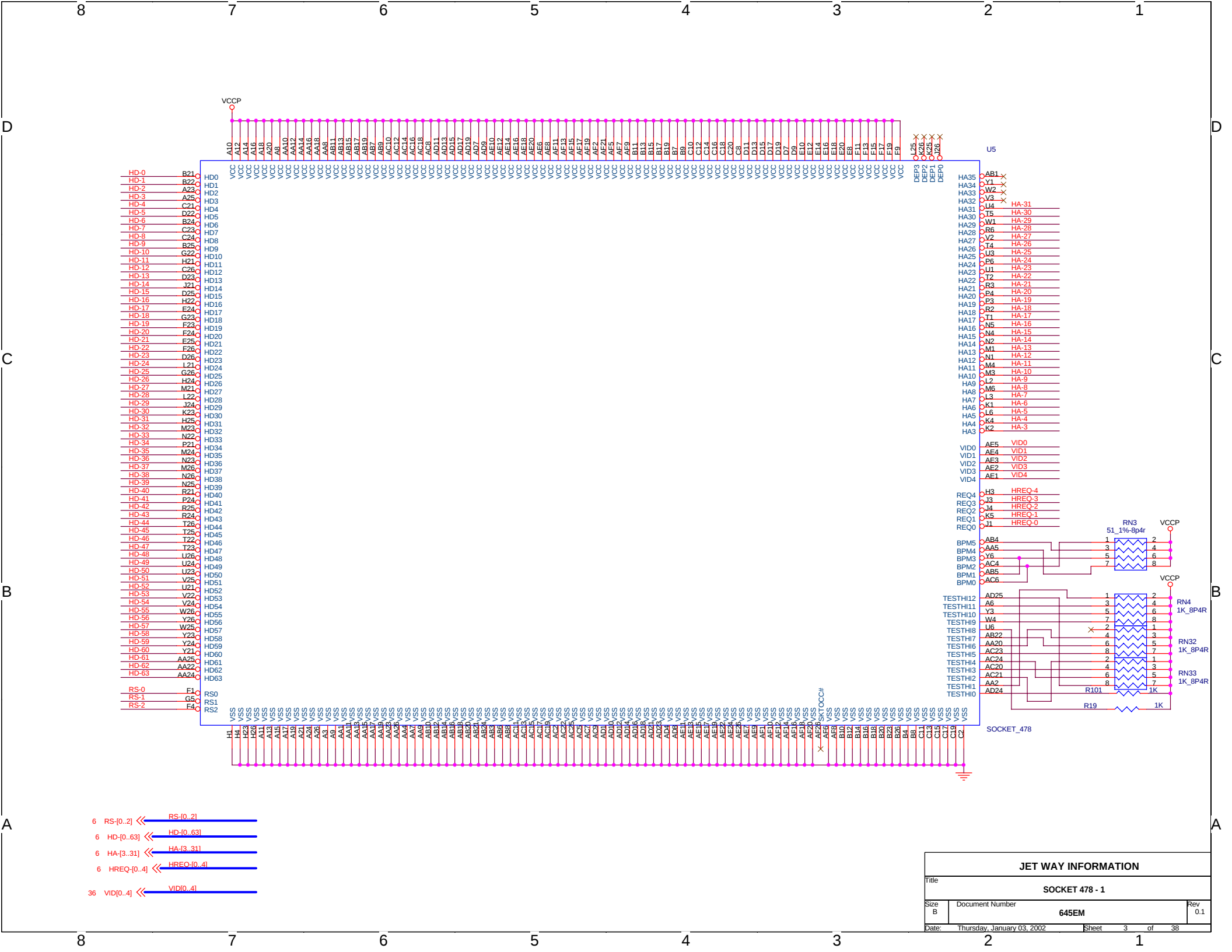
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System Block Diagram



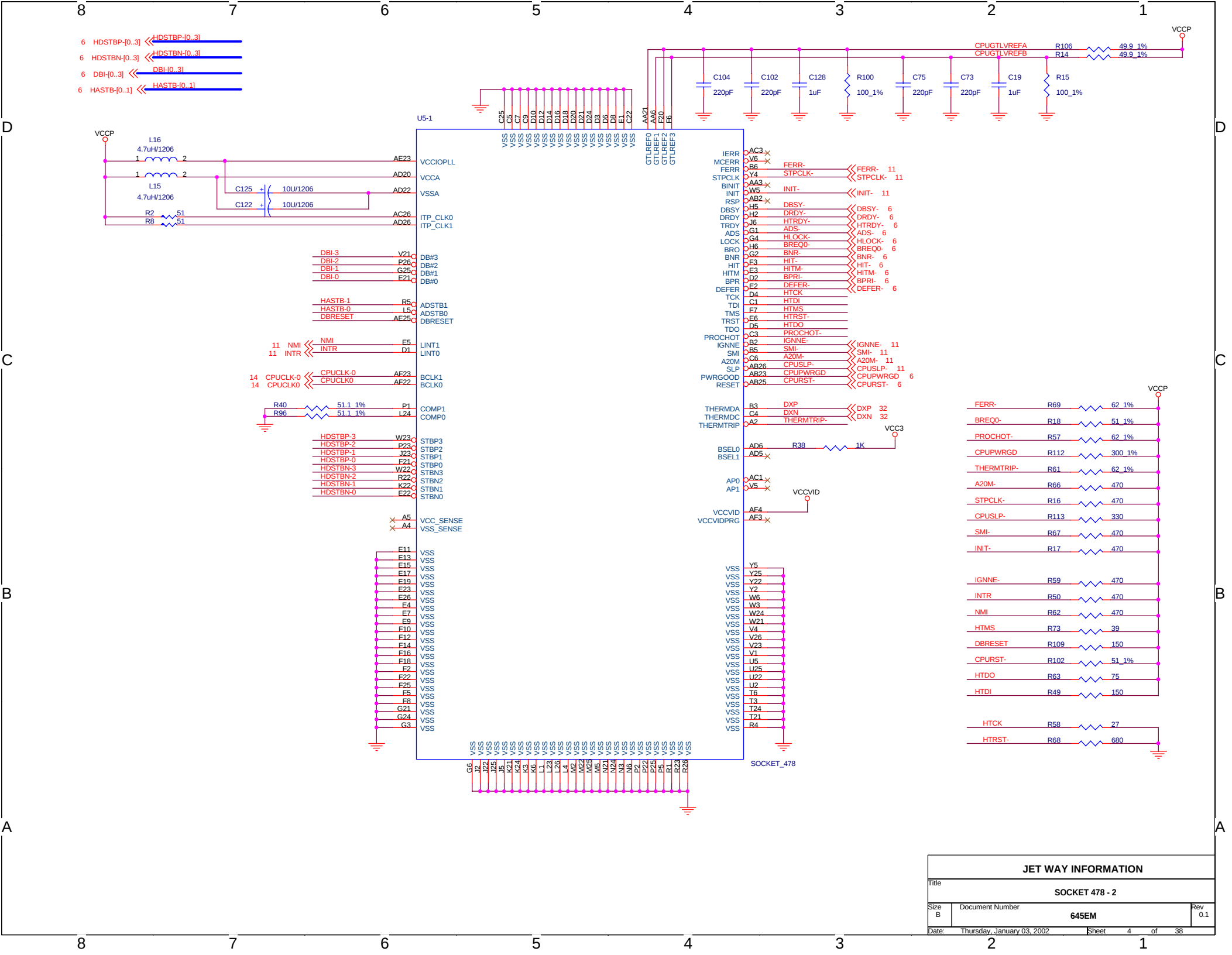
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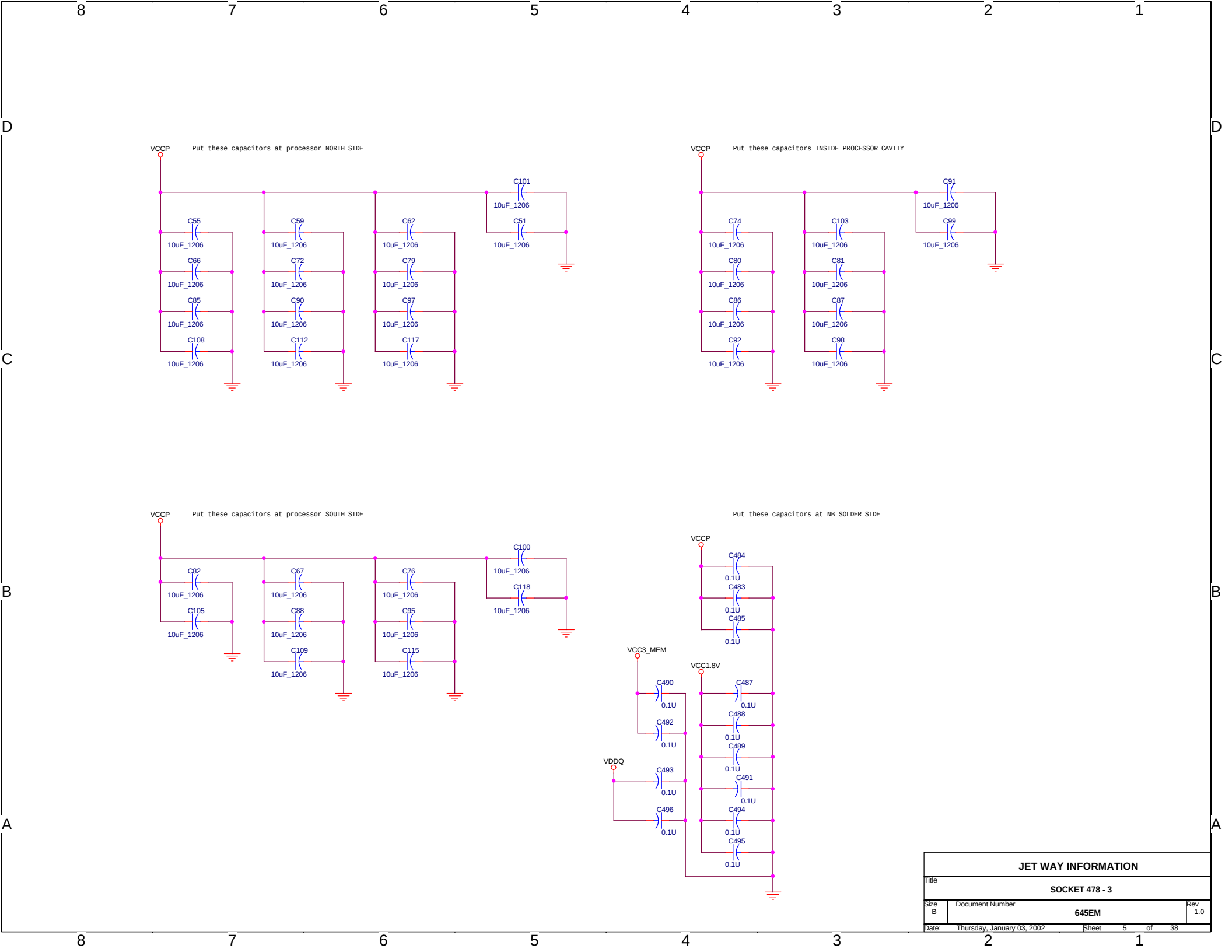
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System Block Diagram			
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6 RS-[0..2] << RS-[0..2]
6 HD-[0..63] << HD-[0..63]
6 HA-[3..31] << HA-[3..31]
6 HREQ-[0..4] << HREQ-[0..4]
36 VID-[0..4] << VID-[0..4]

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SOCKET 478 - 1				
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650-1

AGP

HOST

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645/650-1 (HOST/AGP)			
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18 MA[0..14] << MA[0..14]
18 MD[0..63] << MD[0..63]
18 DQM[0..7] << DQM[0..7]

Rs place close to DIMM1

CKE[0..3] << CKE[0..3] 18,19

U11-1

MD0	AJ23	MD0	AJ23
MD1	AG22	MD1	AG22
MD2	AH21	MD2	AH21
MD3	AJ21	MD3	AJ21
MD4	AD23	MD4	AD23
MD5	AE23	MD5	AE23
MD6	AF22	MD6	AF22
MD7	AF21	MD7	AF21
DQM0	AD22	DQM0	AD22
DQS0	AH22	DQS0/CSB#0	AH22
MD8	AG20	MD8	AG20
MD9	AE19	MD9	AE19
MD10	AF19	MD10	AF19
MD11	AE21	MD11	AE21
MD12	AD20	MD12	AD20
MD13	AD19	MD13	AD19
MD14	AH19	MD14	AH19
MD15	AE20	MD15	AE20
DQM1	AH20	DQM1	AH20
DQS1	AF18	DQS1/CSB#1	AF18
MD16	AG18	MD16	AG18
MD17	AH17	MD17	AH17
MD18	AD16	MD18	AD16
MD19	AD17	MD19	AD17
MD20	AE17	MD20	AE17
MD21	AJ17	MD21	AJ17
MD22	AE17	MD22	AE17
MD23	AJ17	MD23	AJ17
DQM2	AH18	DQM2	AH18
DQS2	AD14	DQS2/CSB#2	AD14
MD24	AG14	MD24	AG14
MD25	AJ13	MD25	AJ13
MD26	AE13	MD26	AE13
MD27	AJ15	MD27	AJ15
MD28	AE14	MD28	AE14
MD29	AD13	MD29	AD13
MD30	AH13	MD30	AH13
MD31	AD10	MD31	AD10
DQM3	AH10	DQM3	AH10
DQS3	AE9	DQS3/CSB#3	AE9
MD32	AD8	MD32	AD8
MD33	AG10	MD33	AG10
MD34	AE10	MD34	AE10
MD35	AD9	MD35	AD9
MD36	AE9	MD36	AE9
MD37	AD9	MD37	AD9
MD38	AE9	MD38	AE9
MD39	AD9	MD39	AD9
DQM4	AH9	DQM4	AH9
MD40	AE5	MD40	AE5
MD41	AG4	MD41	AG4
MD42	AH3	MD42	AH3
MD43	AE4	MD43	AE4
MD44	AD4	MD44	AD4
MD45	AE4	MD45	AE4
MD46	AD4	MD46	AD4
MD47	AE4	MD47	AE4
DQM5	AH4	DQM5	AH4
MD48	AE4	MD48	AE4
MD49	AD6	MD49	AD6
MD50	AE2	MD50	AE2
MD51	AC5	MD51	AC5
MD52	AG2	MD52	AG2
MD53	AG1	MD53	AG1
MD54	AE3	MD54	AE3
MD55	AC6	MD55	AC6
DQM6	AD4	DQM6	AD4
MD56	AE2	MD56	AE2
MD57	AD3	MD57	AD3
MD58	AA6	MD58	AA6
MD59	AB3	MD59	AB3
MD60	AC4	MD60	AC4
MD61	AE1	MD61	AE1
MD62	AD2	MD62	AD2
MD63	AC1	MD63	AC1
DQM7	AB4	DQM7	AB4
MD64	AC2	MD64	AC2

650

Rs place close to DIMM1

MA0 AH11 MA0
MA1 AH12 MA1
MA2 AG12 MA2
MA3 AD12 MA3
MA4 AH15 MA4
MA5 AF15 MA5
MA6 AE15 MA6
MA7 AH16 MA7
MA8 AE15 MA8
MA9 AD15 MA9
MA10 AE11 MA10
MA11 AG8 MA11
MA12 AJ11 MA12
MA13 AG16 MA13
MA14 AE16 MA14

SRAS# SRAS- 18
SCAS# SCAS- 18
SWE# SWE- 18

CS#0 AE7 CS-0 18
CS#1 AE7 CS-1 18
CS#2 AH6 CS-2 18
CS#3 AJ5 CS-3 18
CS#4 AE8 CS-3 18
CS#5 AD7 CS-3 18

CKE0 AB2 CKE0
CKE1 AA4 CKE1
CKE2 AB1 CKE2
CKE3 Y6 CKE3
CKE4 AA5 CKE4
CKE5 Y5 CKE5

S3AUXSW# Y4 S3AUXSW- 37

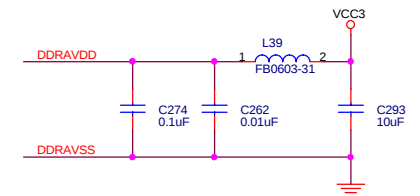
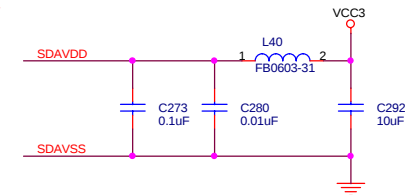
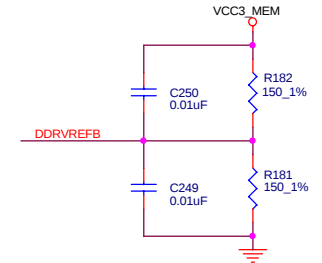
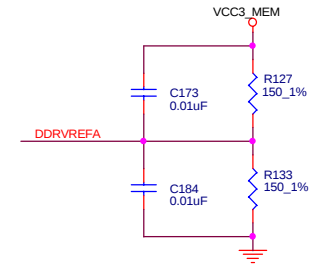
SDCLK AA3 SDCLK 14
FWDSDCLKO AD11 R151 0 FWDSDCLKO 15
SDRCLKI AE11 SDCLKI 15

SDAVDD Y1 SDAVDD
SDAVSS Y2 SDAVSS

DDRAVDD AA1 DDRAVDD
DDRAVSS AA2 DDRAVSS

DDRVREFA AJ19 DDRVREFA
DDRVREFB AH2 DDRVREFB

DRAM_SEL W3 R211 4.7K



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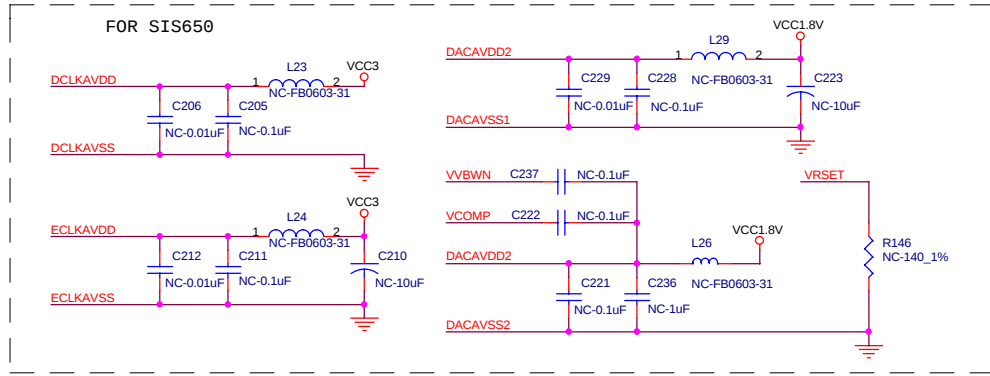
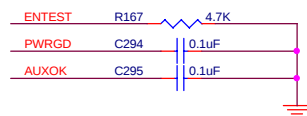
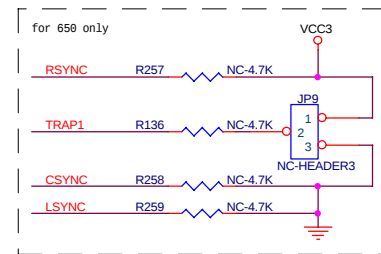
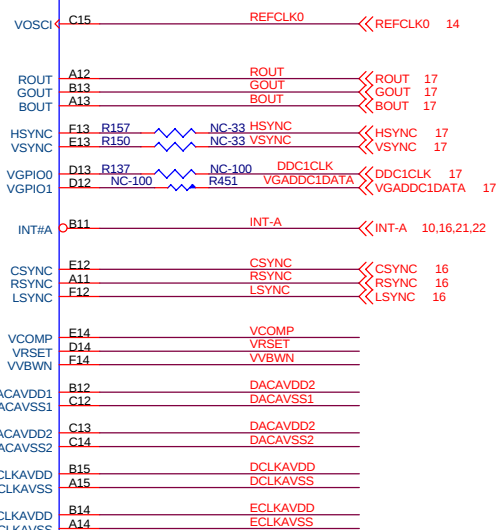
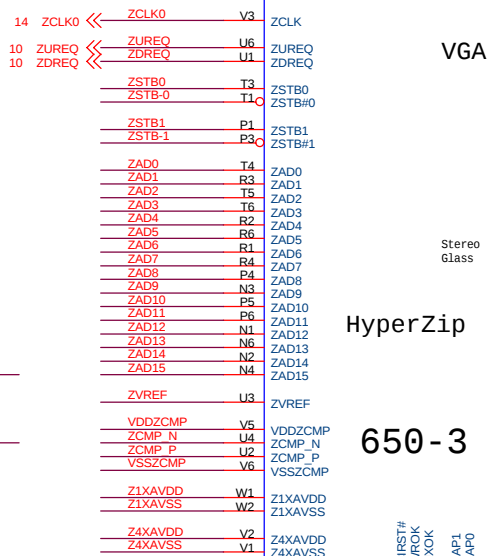
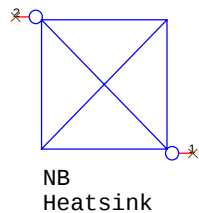
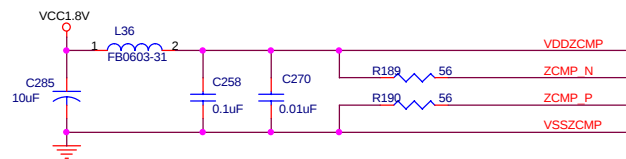
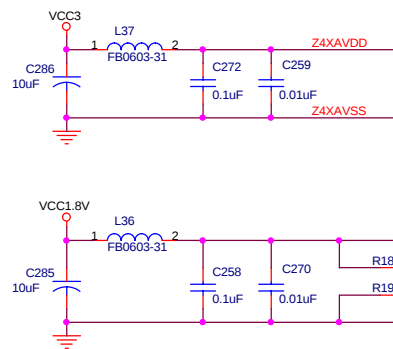
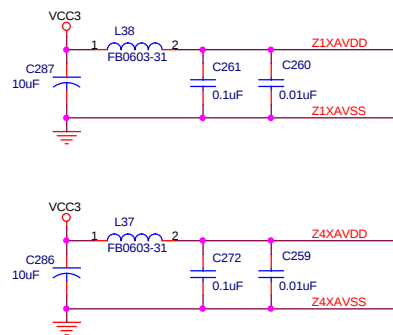
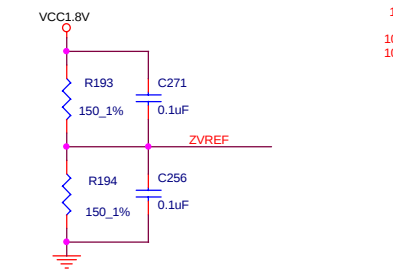
Title			
645/650-2 (MEMORY for SDR)			
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10 ZAD[0..15] << ZAD[0..15]
10 ZSTB[0..1] << ZSTB[0..1]
10 ZSTB[0..1] << ZSTB[0..1]

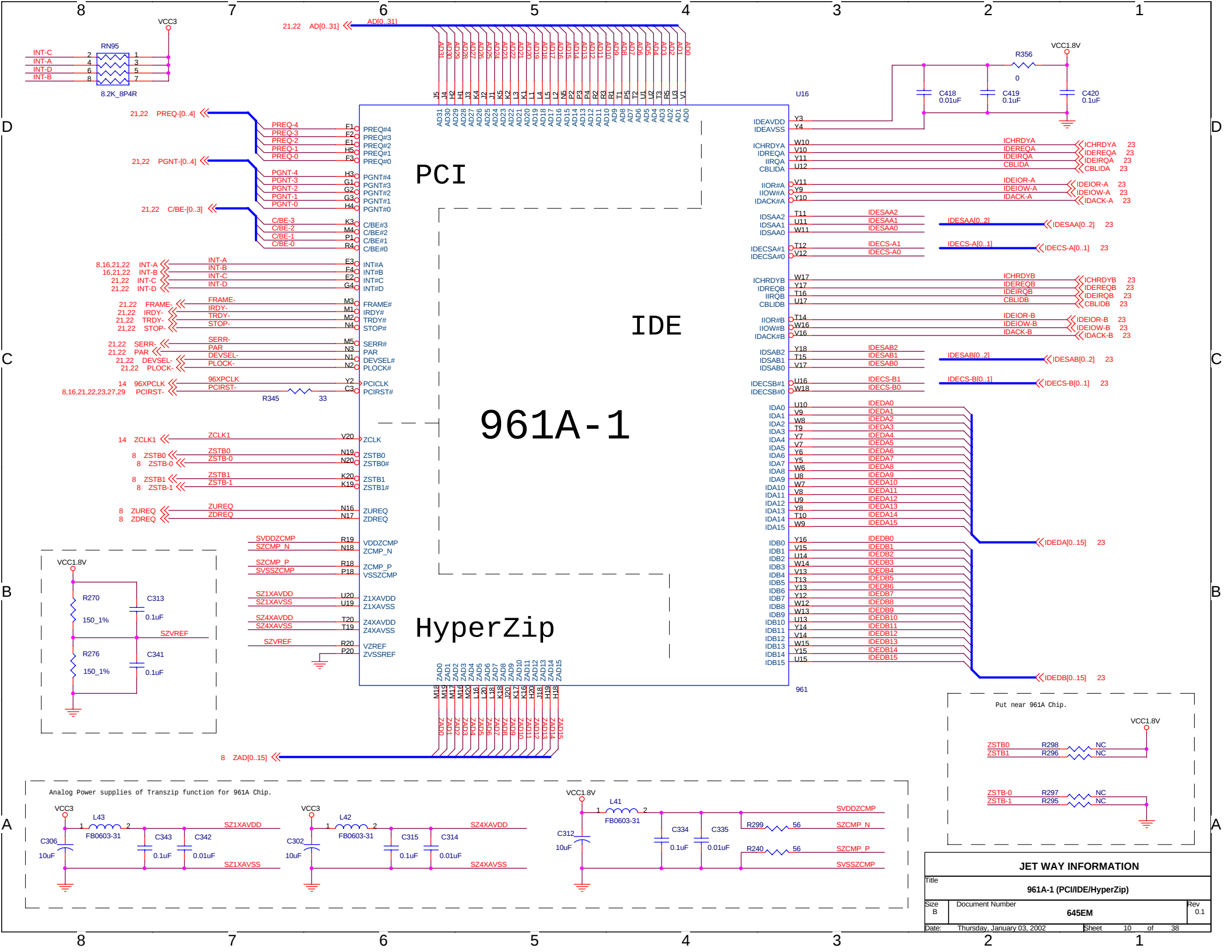
NOTE: This page is for universal PCB design(suitable for both 645 or 650)

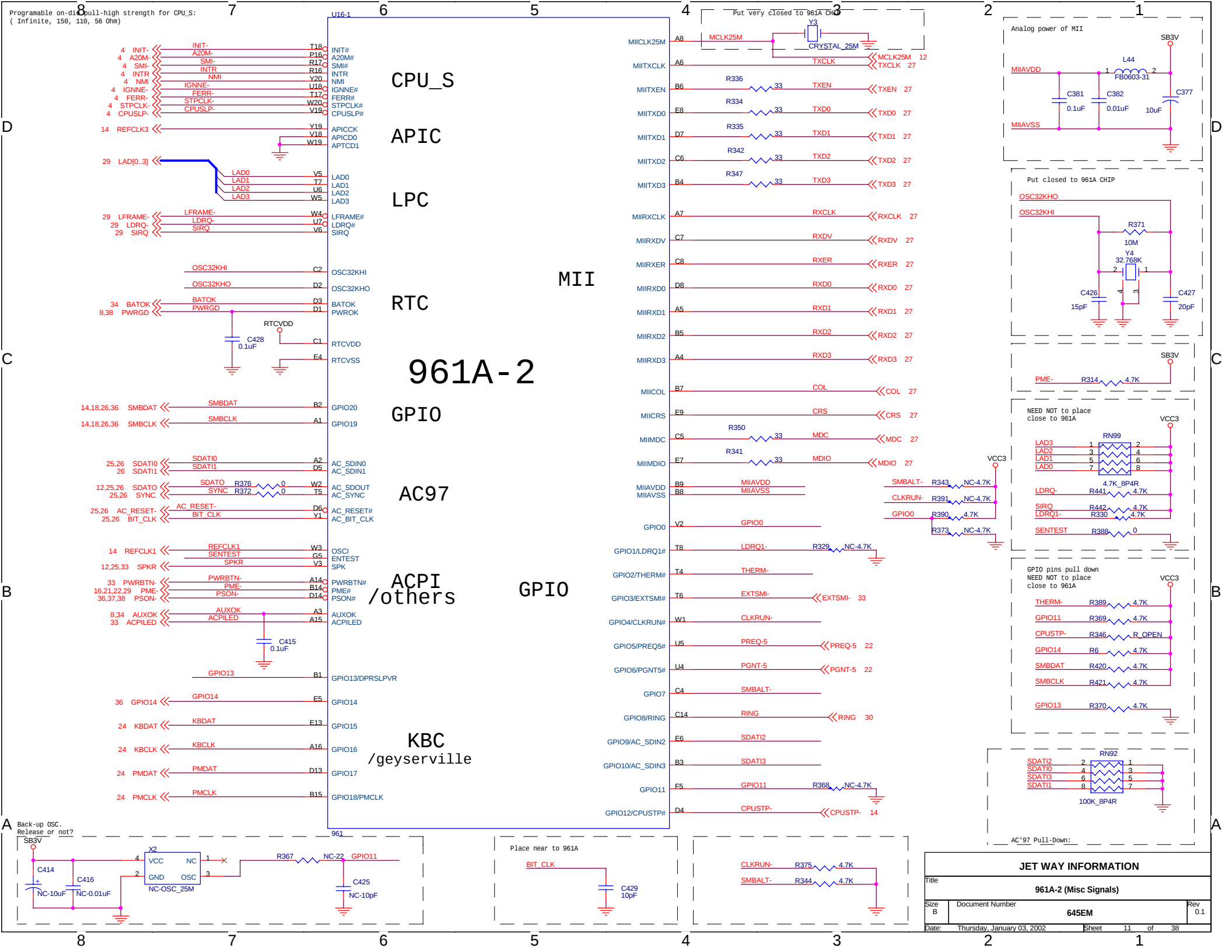
NB Hardware Trap Table

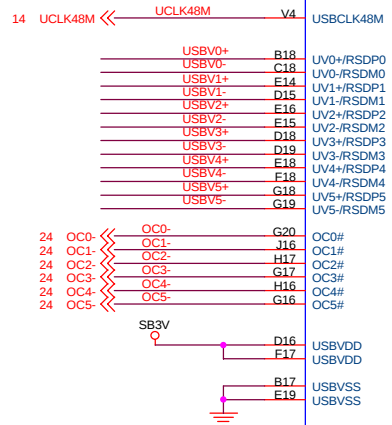
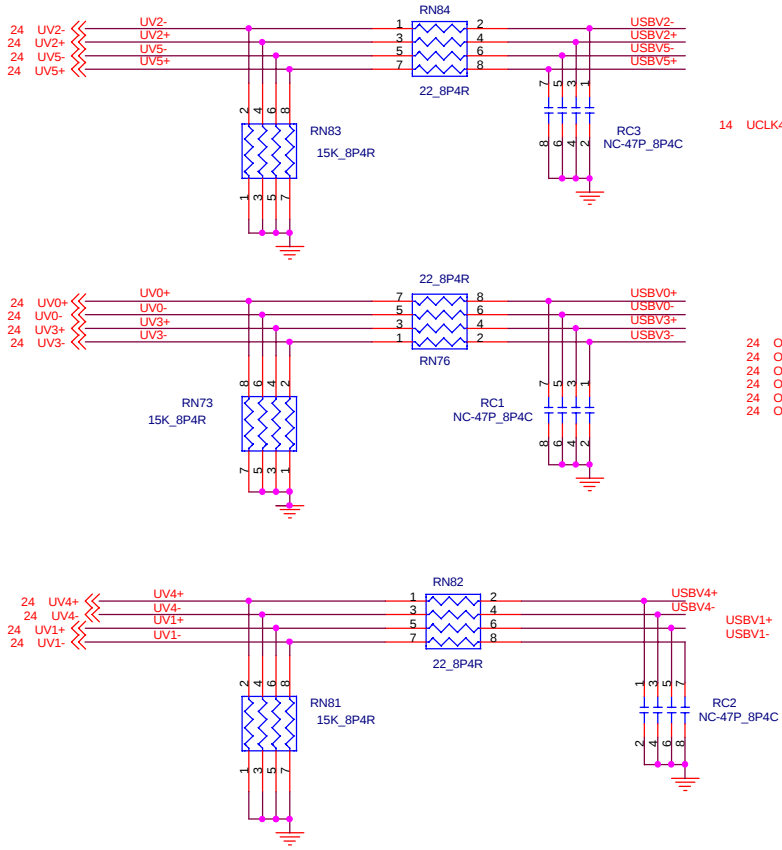
PLLEN#	enable	0	1	Default	embedded pull-low (30-50K Ohm)
DRAM_SEL	SOR	normal	disable PLL	yes	yes
TRAP0			DOR	1(DDR)	yes
			Nb debug mode	0	
TRAP1	TV selection, NTSC/PAL(0/1)			0	
CSYNC	enable VB			0	
RSYNC	enable VGA interface			1	
LSYNC	enable panel link			0	



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645/650-3 (HyperZip/Others)			
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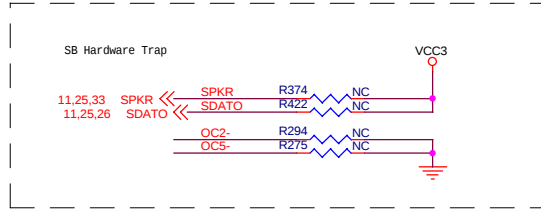
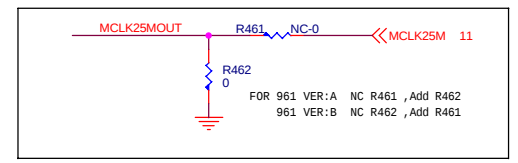






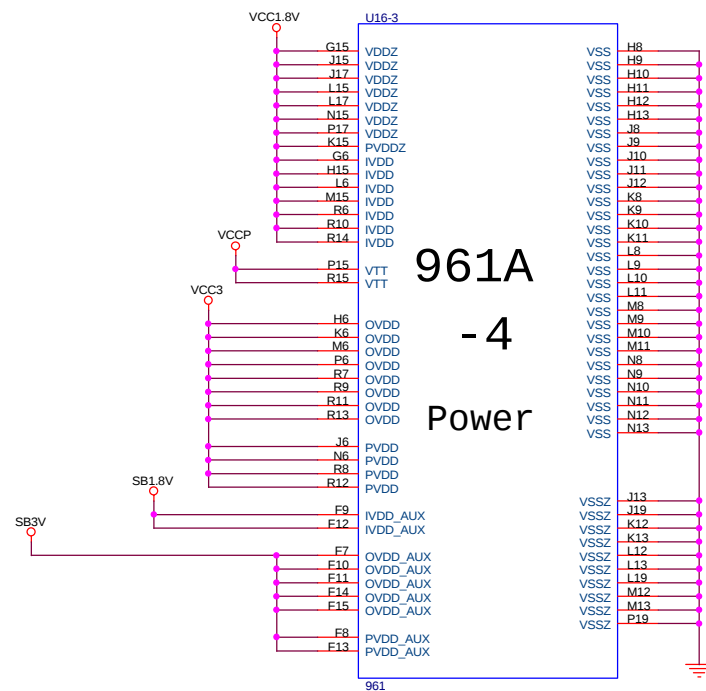
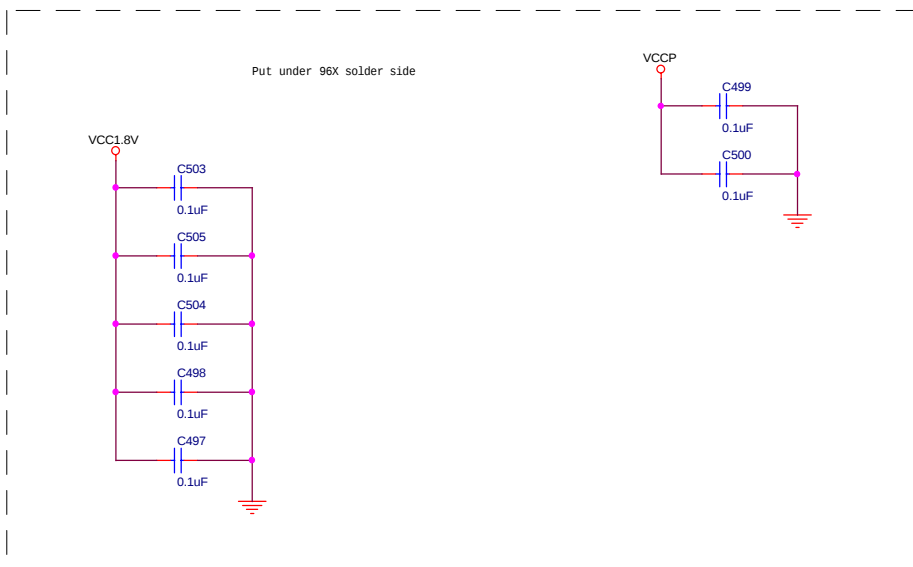
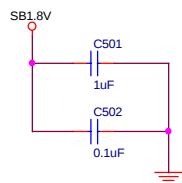
USB

961A-3



	0	1	Default	embedded pull-low (30-50K Ohm)
SPKR(LPC_addr mapping)	disable	enable	0	yes
SDATO(PCICLK_PLL)	enable	disable	0	yes
OC2-(SB debug mode)	enable	disable	1	yes
OC5-(Trap mode)	PCI_AD	ROM	1	yes

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Title			
961A-4 (Powers)			
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Main Clock Generator

(3 OPTIONS)
1: (ICS: ICS952001)
2: (Cypress: CY28342)
3: (Hitachi: HDT5463)

CPUCLK=645CPUCLK=SDCLK
AGPCLK0=AGPCLK1+3.3"
ZCLK0=ZCLK1
PCICK0=PCICK1
PCICK1=PCICK2=PCICK3

By-Pass Capacitors
Place near to the Clock Outputs

Damping Resistors
Place near to the
Clock Outputs

CPUCLK0 R197 49.9 1%
CPUCLK-0 R198 49.9 1%
CPUCLK1 R195 49.9 1%
CPUCLK-1 R196 49.9 1%

SDCLK C263 10pF
AGPCLK0 C265 10pF
AGPCLK1 C266 10pF
ZCLK0 C362 10pF
ZCLK1 C363 10pF
96XPCLK C364 10P

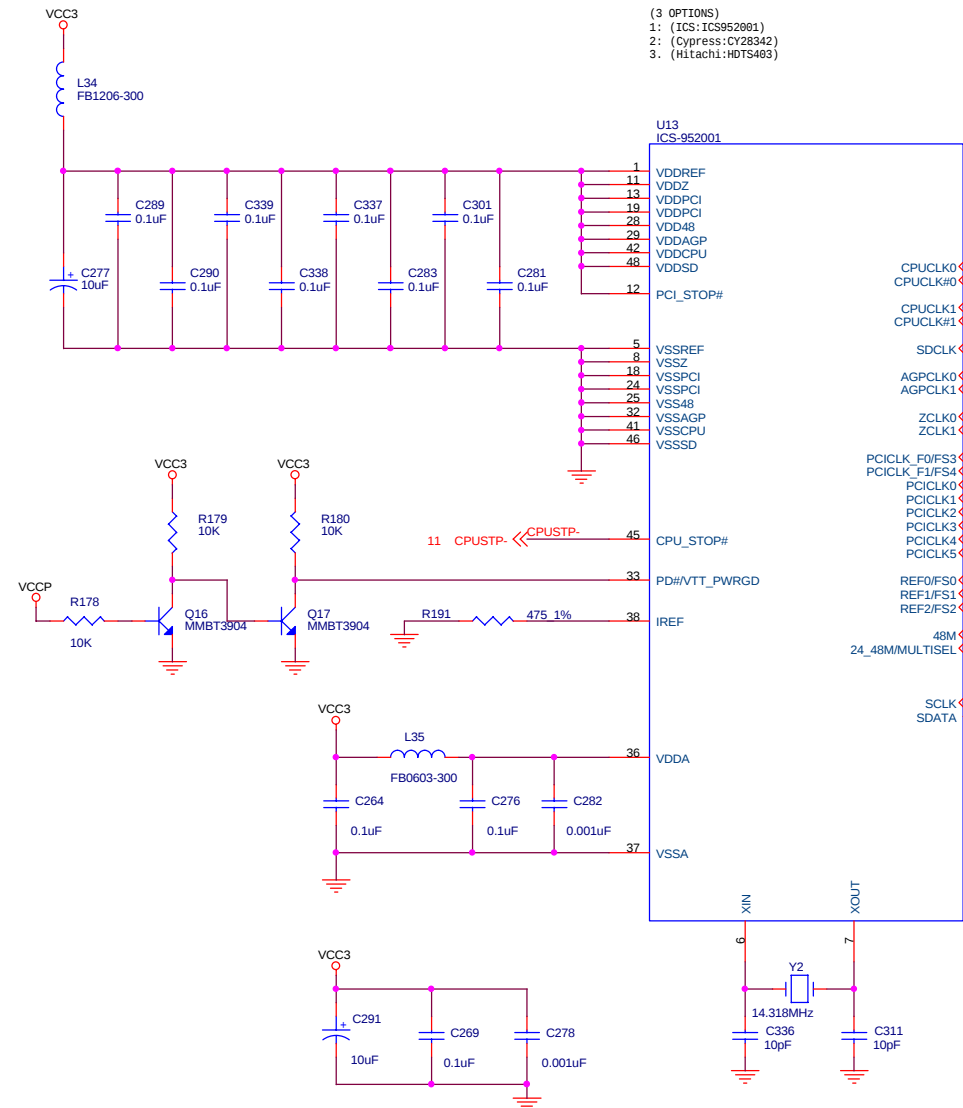
SIOPCLK CN13 2 1 10P 8P4C
PCICK1 4 3
PCICK2 6 5
PCICK3 8 7

REFCLK0 C358 NC-10pF
REFCLK1 C359 10pF
REFCLK2 C361 10pF
REFCLK3 C360 10pF
UCLK48M C267 10pF
SIO48M C268 10pF

Frequency Selection

ON=1
OFF=0

MULTISEL R199 R_OPEN



SIS650 CLOCK											SIS650 CLOCK										
FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)		FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	
0	0	0	0	0	66.7	66.7	66.7	66.7	33.33		1	0	0	0	0	105.00	140.00	70.00	70.00	35.00	
0	0	0	0	1	100.00	100.00	66.7	66.7	33.33		1	0	0	0	1	100.00	100.00	67.27	67.27	33.63	
0	0	0	1	0	100.00	200.00	66.7	66.7	33.33		1	0	0	1	0	100.00	144.00	72.00	72.00	36.00	
0	0	0	1	1	100.00	133.33	66.7	66.7	33.33		1	0	0	1	1	100.00	134.53	67.27	67.27	33.63	
0	0	1	0	0	100.00	150.00	60.00	60.00	30.00		1	0	1	0	0	112.00	149.33	74.67	74.67	37.33	
0	0	1	0	1	100.00	125.00	62.50	62.50	31.25		1	0	1	0	1	133.33	100.00	66.67	66.67	33.33	
0	0	1	1	0	100.00	160.00	66.67	66.67	33.33		1	0	1	1	0	133.33	133.33	66.67	66.67	33.33	
0	0	1	1	1	100.00	133.33	80.00	66.67	33.33		1	0	1	1	1	133.33	166.67	66.67	66.67	33.33	
0	1	0	0	0	100.00	200.00	66.67	66.67	33.33		1	1	0	0	0	100.00	133.33	80.00	66.67	33.33	
0	1	0	0	1	100.00	166.67	62.50	62.50	31.25		1	1	0	1	0	100.00	100.00	66.67	66.67	33.33	
0	1	0	1	0	100.00	166.67	71.43	83.33	41.67		1	1	0	1	0	100.00	166.67	83.33	62.50	31.25	
0	1	0	1	1	100.00	133.33	66.67	66.67	33.33		1	1	0	1	1	133.33	160.00	80.00	66.67	33.33	
0	1	1	0	0	80.00	133.33	66.67	66.67	33.33		1	1	1	0	0	100.00	133.00	100.00	66.67	33.33	
0	1	1	1	0	95.00	95.00	63.33	63.33	31.67		1	1	1	1	0	100.00	100.00	100.00	66.67	33.33	
0	1	1	1	1	95.00	126.67	63.33	63.33	31.67		1	1	1	1	1	100.00	166.67	100.00	62.50	31.25	
0	1	1	1	1	66.67	66.67	50.00	50.00	25.00		1	1	1	1	1	133.33	100.00	100.00	66.67	33.33	

JET WAY INFORMATION

Title				MAIN CLOCK GENERATOR (3 OPTIONS)			
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Clock Buffer (SDR)

SDCLKI0..71 << SDCLK[0..7] 18

FWDSCLKO << FWDSCLKO 7

By-Pass Capacitors
Place near to the Clock Buffer

SDCLK0 2 1
SDCLK1 4 3
SDCLK2 6 5
SDCLK3 8 7

NC-10_8P4C

SDCLK4 2 1
SDCLK5 4 3
SDCLK6 6 5
SDCLK7 8 7

NC-10P_8P4C

FB_OUT 10pF C31
FWDSCLKO C16 NC-10P

FB_OUT=SDRCLK+FWDSCLKO - AVGMA -1.9"
SDCLKI=SDRCLK+AVGMA+1.5"

CLK1 ICS9179BF-19

VDD 5 11 15 20 25
CBVDD3

VCC3 L5 FB0603-300

C24 10uF
C25 0.1uF
C30 0.01uF

VDDA 16
GNDA 17

FWDSCLKO 6
FB_OUT 7

INPUT 6
FB_IN 7

CLK0 3
CLK1 4
CLK2 9
CLK3 10
CLK4 13
CLK5 14

SDCLK0 1
SDCLK1 3
SDCLK2 5
SDCLK3 7

0_8P4R RN1

CLK4 18
CLK5 19
CLK6 26
CLK7 27

SDCLK4 1
SDCLK5 3
SDCLK6 5
SDCLK7 7

0_8P4R RN5

VDDF 23
CBVDD3

OE 1
R9 4.7K
CBVDD3

FB_OUT 22
R36

FB_OUT 22

VCC3 L1 FB1206-300

C4 22uF
C5 0.1uF
C10 0.01uF
C11 0.1uF
C13 0.01uF
C22 0.1uF
C39 0.1uF
C6 22uF

CBVDD3

FB_OUT=SDRCLK+FWDSCLKO - AVGMA -1.9"
SDCLKI=SDRCLK+AVGMA+1.5"

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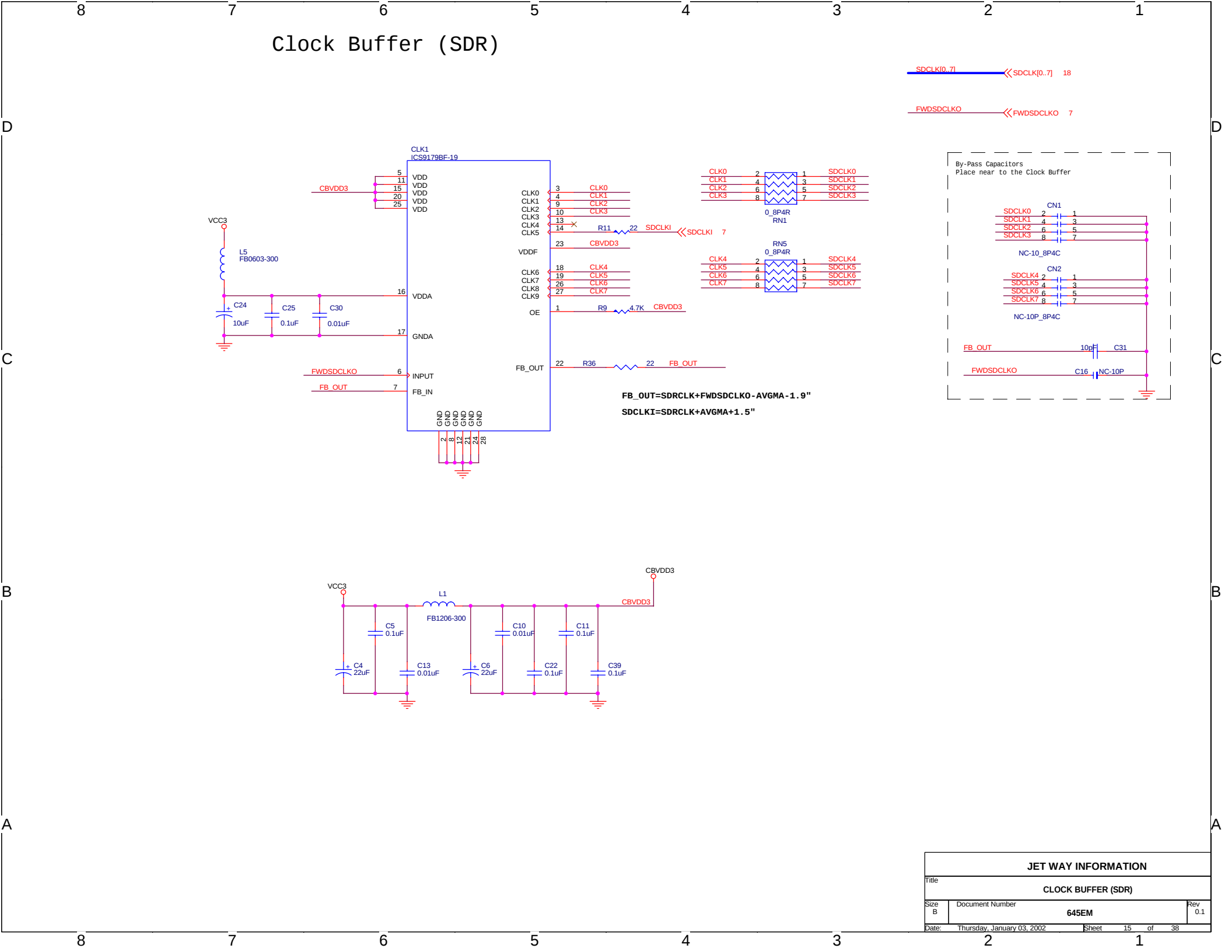
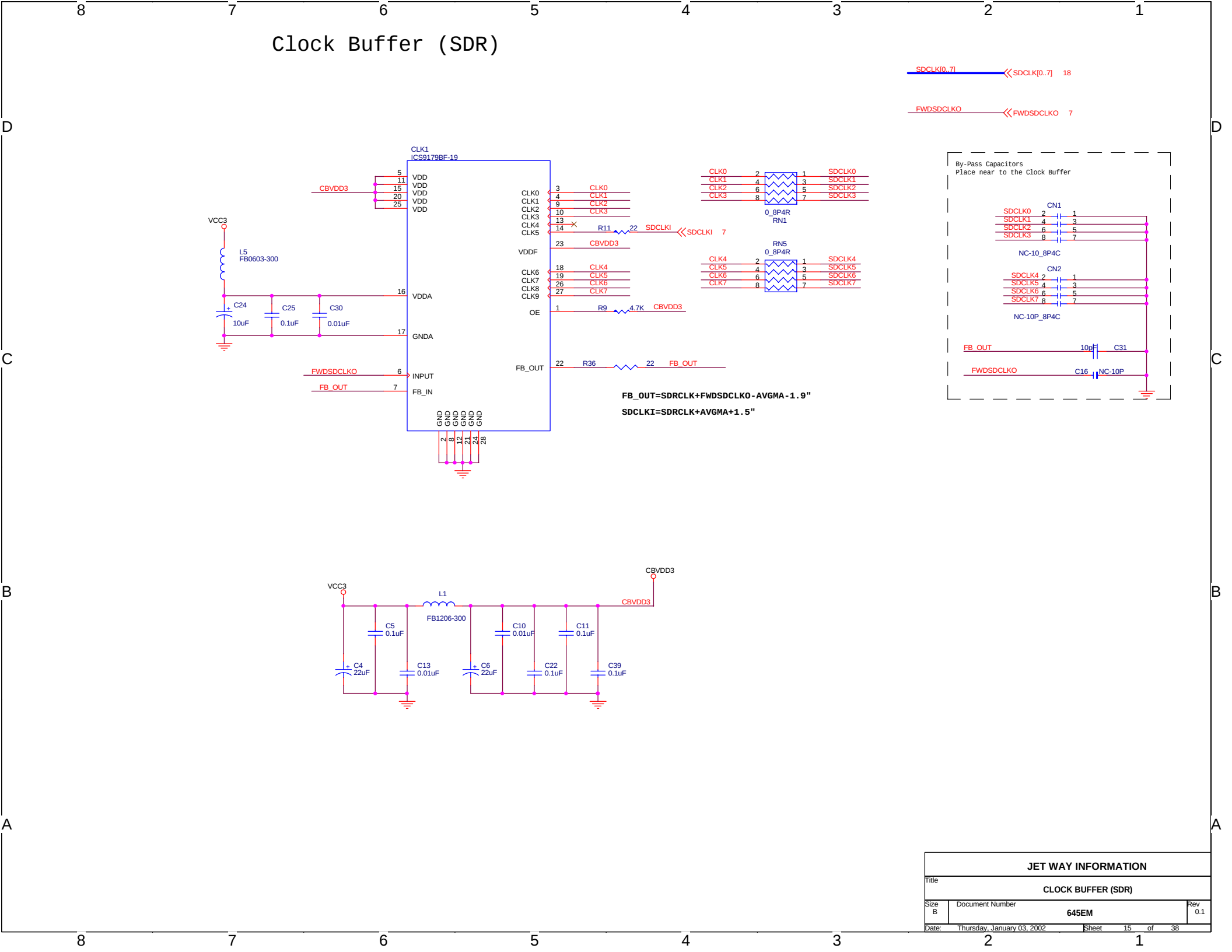
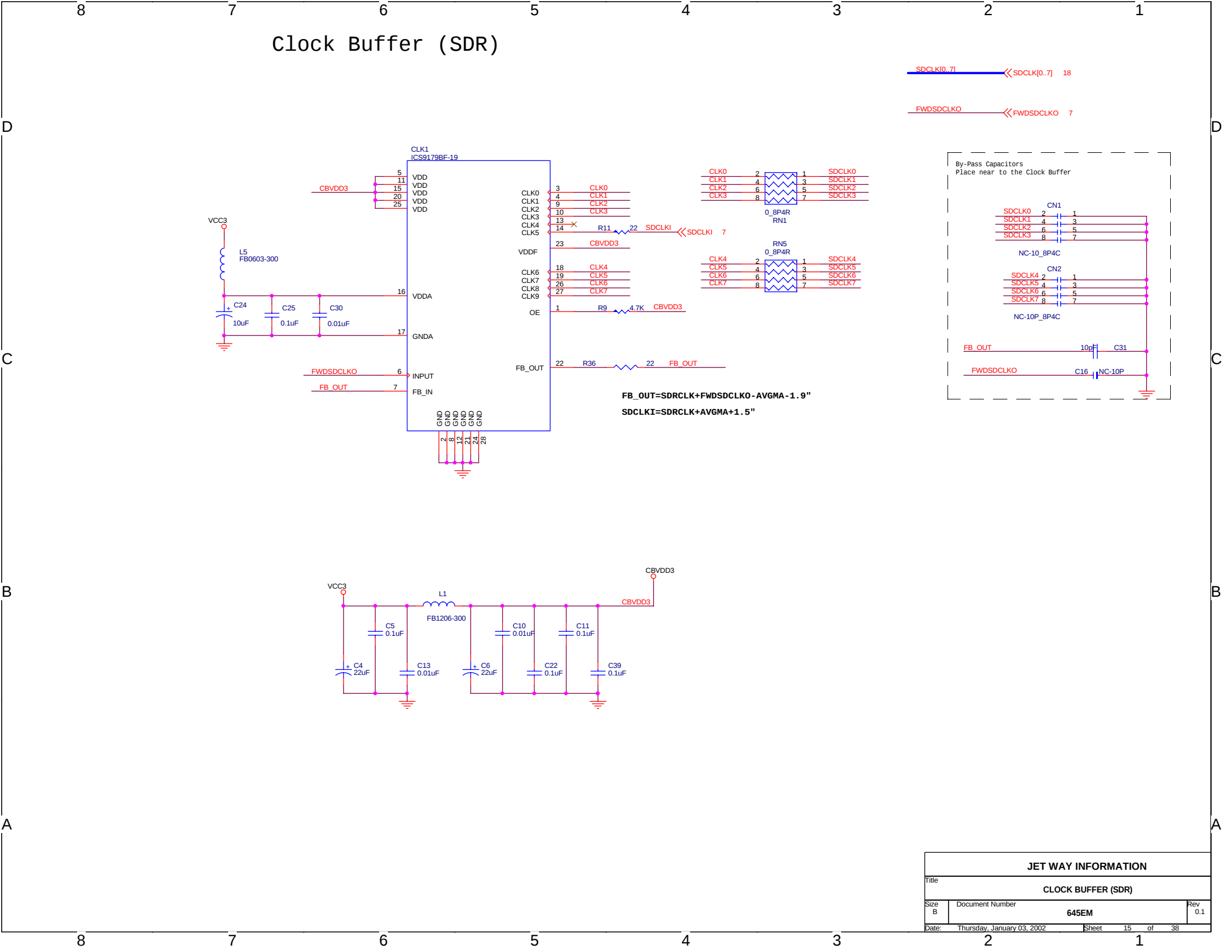
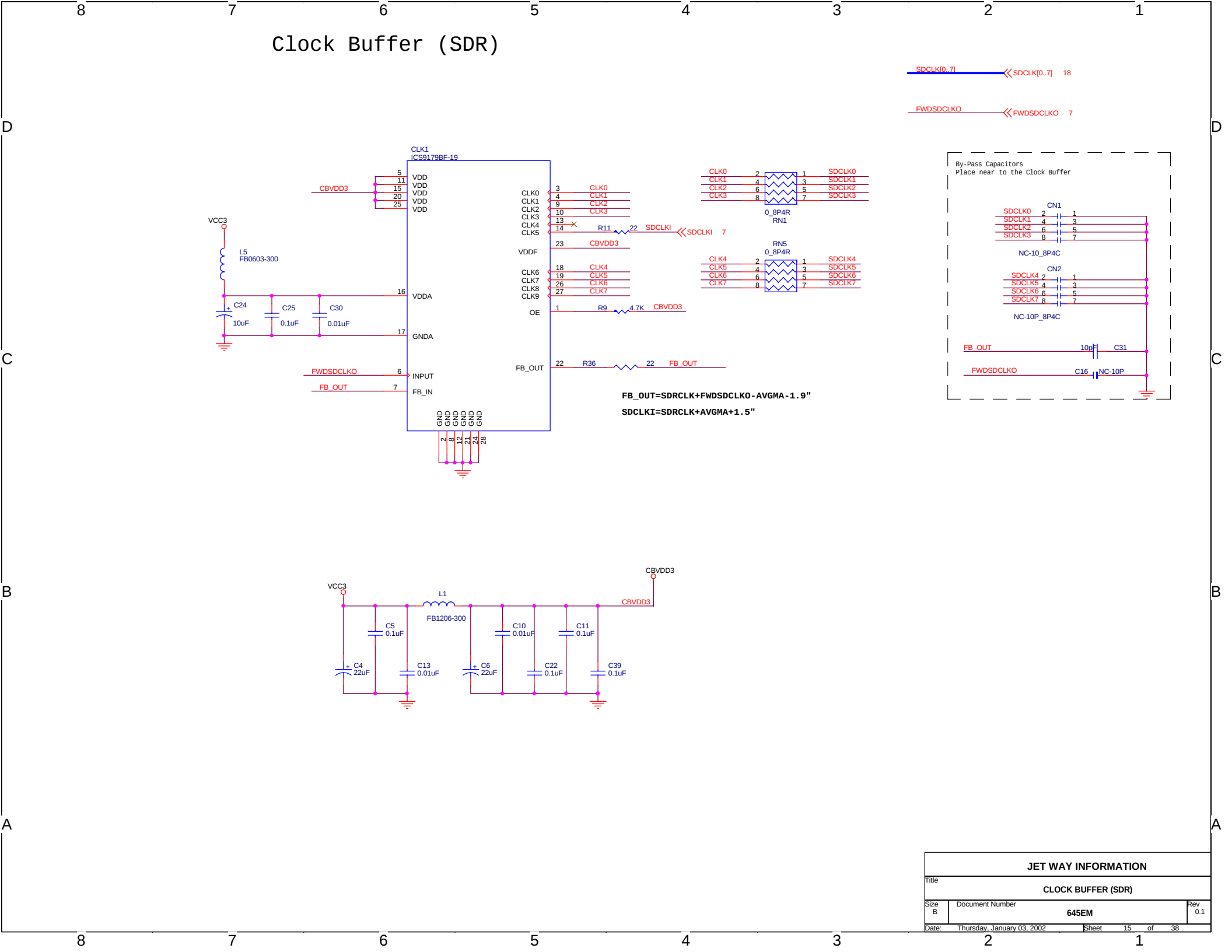
CLOCK BUFFER (SDR)

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Clock Buffer (SDR)

SDCLKI0..71 << SDCLK[0..7] 18

FWDSCLKO << FWDSCLKO 7

By-Pass Capacitors
Place near to the Clock Buffer

SDCLK0 2 1
SDCLK1 4 3
SDCLK2 6 5
SDCLK3 8 7

NC-10_8P4C

SDCLK4 2 1
SDCLK5 4 3
SDCLK6 6 5
SDCLK7 8 7

NC-10P_8P4C

FB_OUT 10pF C31
FWDSCLKO C16 NC-10P

FB_OUT=SDRCLK+FWDSCLKO - AVGMA -1.9"
SDCLKI=SDRCLK+AVGMA+1.5"

CLK1 ICS9179BF-19

CLK0 3 CLK0
CLK1 4 CLK1
CLK2 9 CLK2
CLK3 10 CLK3
CLK4 13 CLK4
CLK5 14 CLK5
CLK6 18 CLK6
CLK7 19 CLK7
CLK8 26 CLK8
CLK9 27 CLK9

VDD 5 VDD
VDD 11 VDD
VDD 15 VDD
VDD 20 VDD
VDD 25 VDD

CBVDD3

VCC3

L5 FB0603-300

C24 10uF
C25 0.1uF
C30 0.01uF

VDDA 16
GNDA 17

FWDSCLKO 6
FB_OUT 7

INPUT 6
FB_IN 7

FB_OUT 22
R36 22

R11 22
SDCLKI << SDCLKI 7

SDCLKI << SDCLKI 7

SDCLK0 2 1
SDCLK1 4 3
SDCLK2 6 5
SDCLK3 8 7

0_8P4R RN1

0_8P4R RN5

CLK4 2 1
CLK5 4 3
CLK6 6 5
CLK7 8 7

SDCLK4 2 1
SDCLK5 4 3
SDCLK6 6 5
SDCLK7 8 7

R9 4.7K
CBVDD3

FB_OUT=SDRCLK+FWDSCLKO - AVGMA -1.9"
SDCLKI=SDRCLK+AVGMA+1.5"

VCC3

CBVDD3

FB1206-300 L1

C5 0.1uF
C10 0.01uF
C11 0.1uF

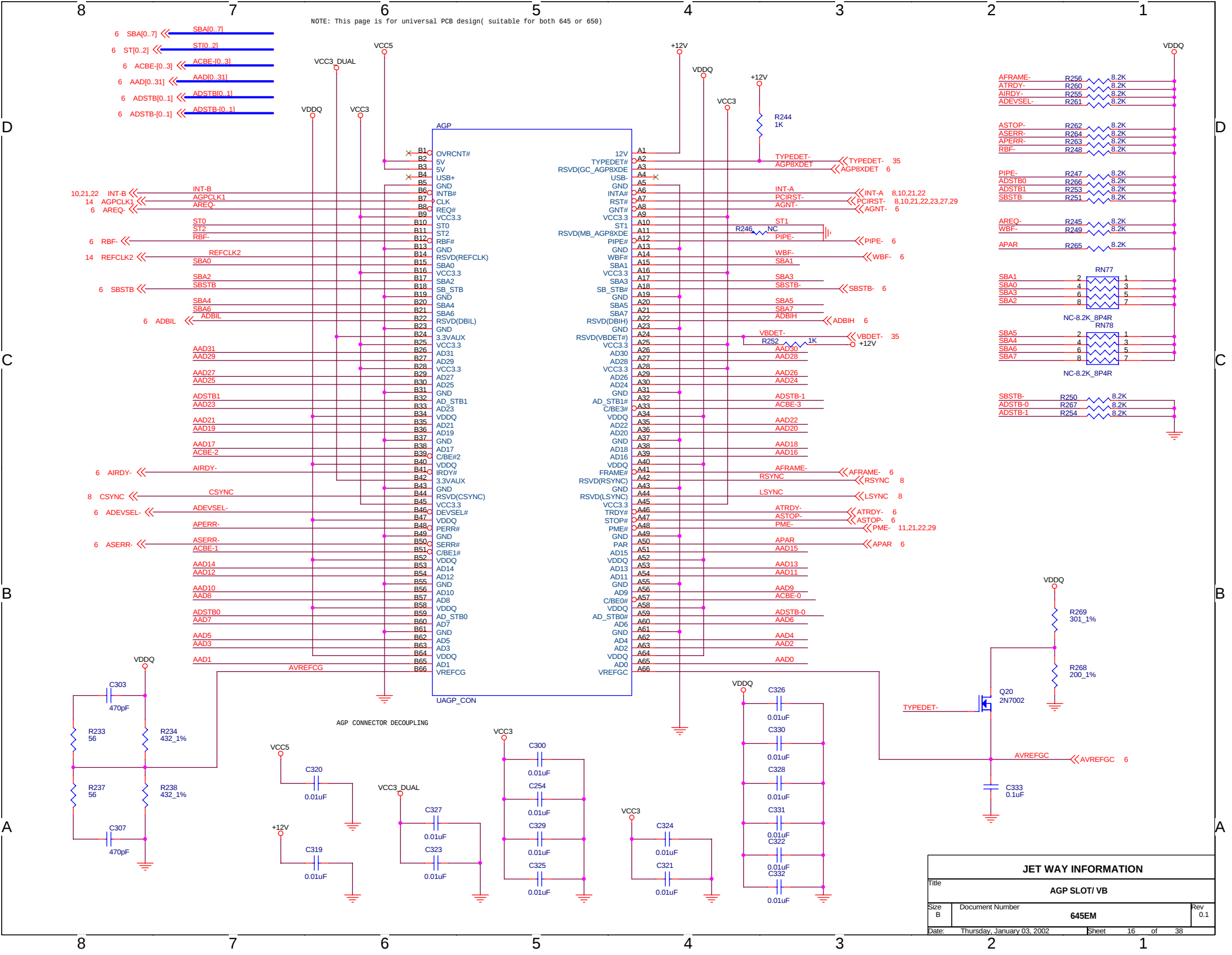
C4 22uF
C13 0.01uF
C6 22uF
C22 0.1uF
C39 0.1uF

JET WAY INFORMATION

Title: **CLOCK BUFFER (SDR)**

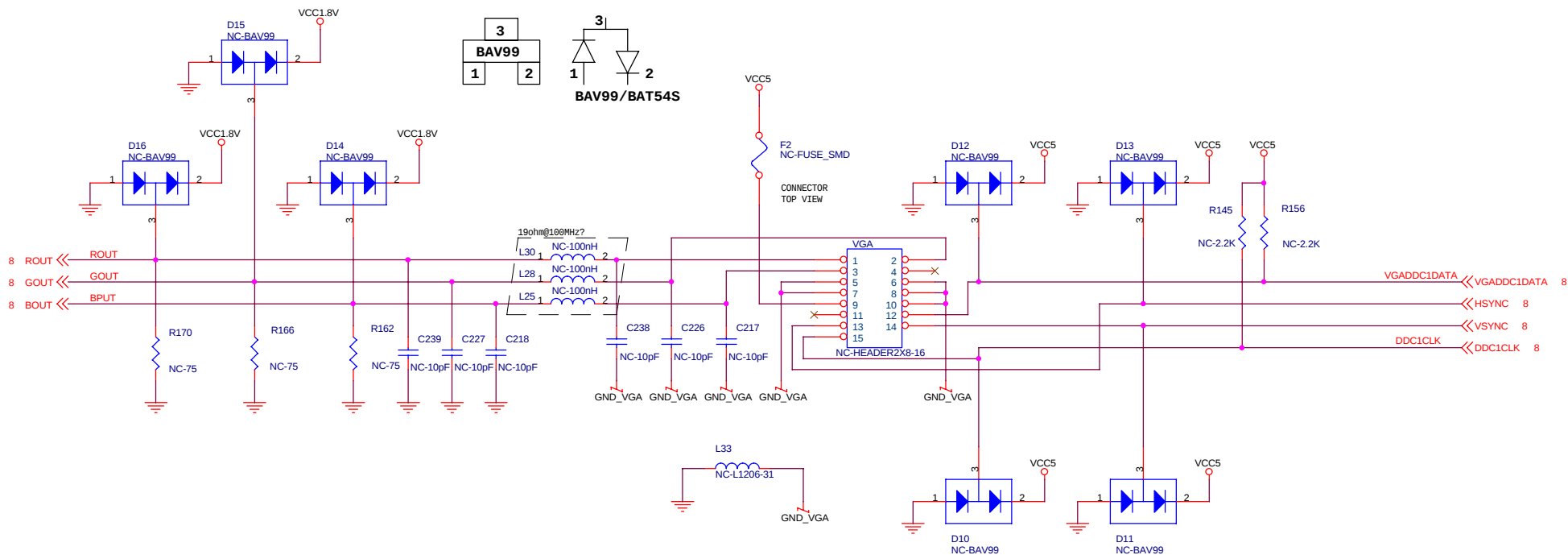
Size: B Document Number: **645EM** Rev: 0.1

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VGA CONNECTOR

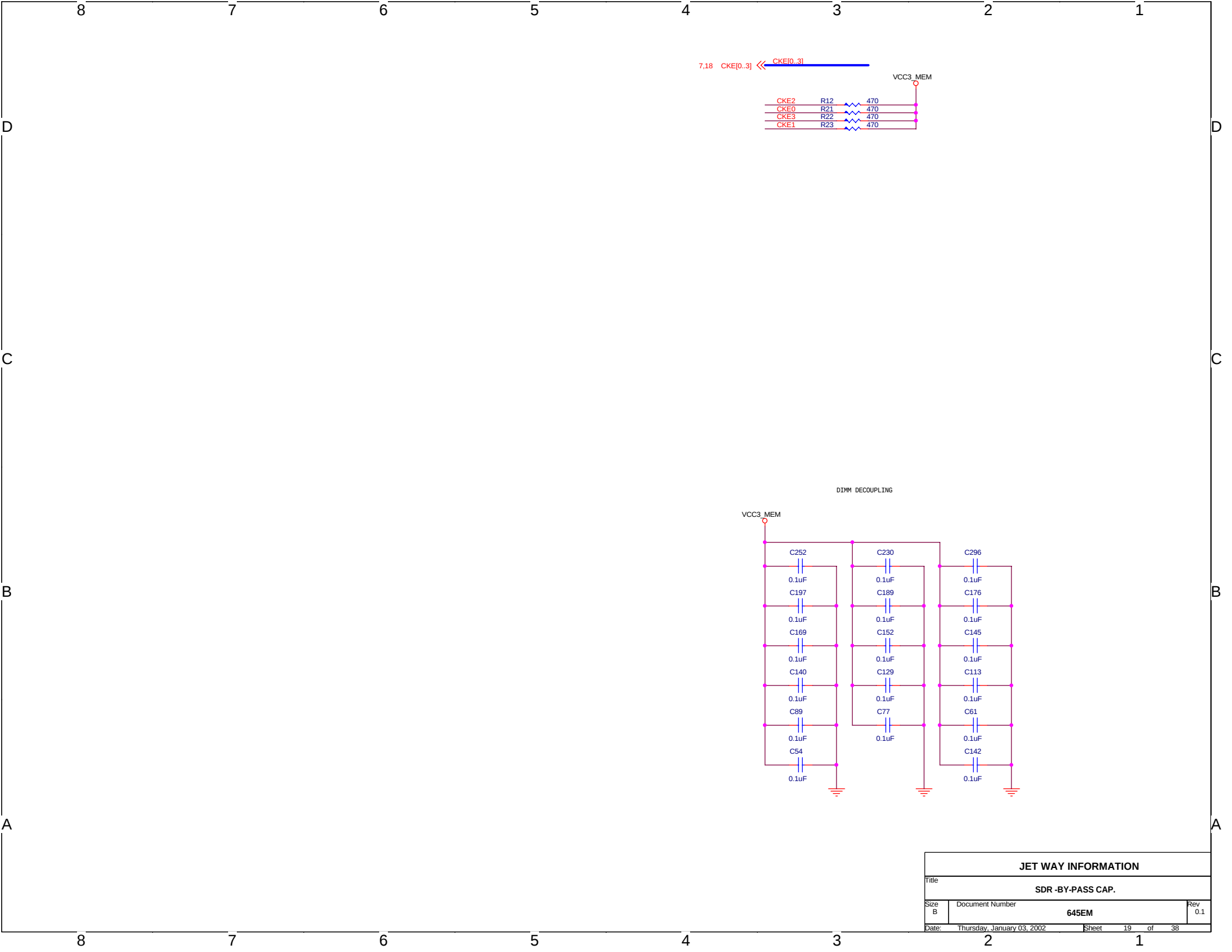
NOTE: This page is for universal PCB design(suitable for both 645 or 650)

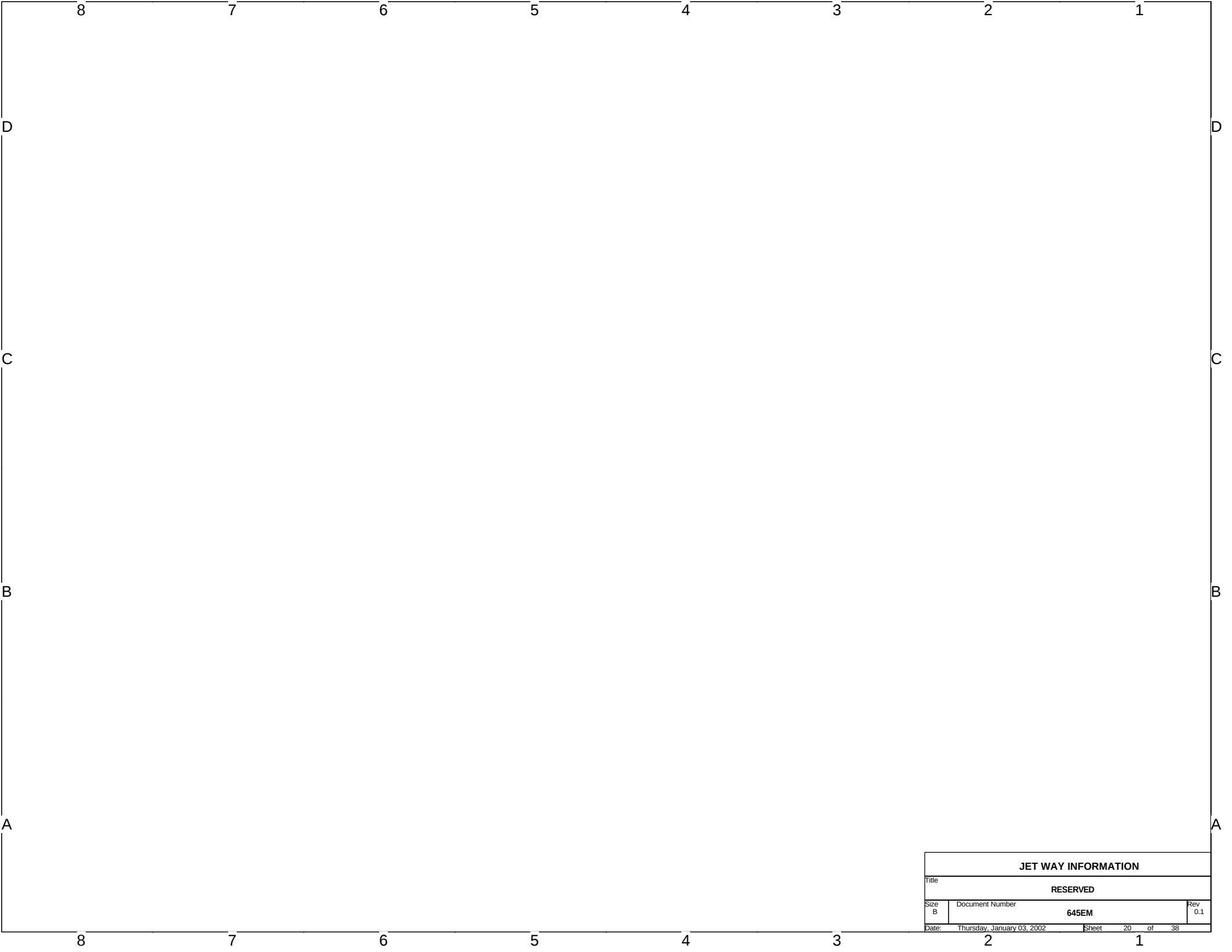


JET WAY INFORMATION

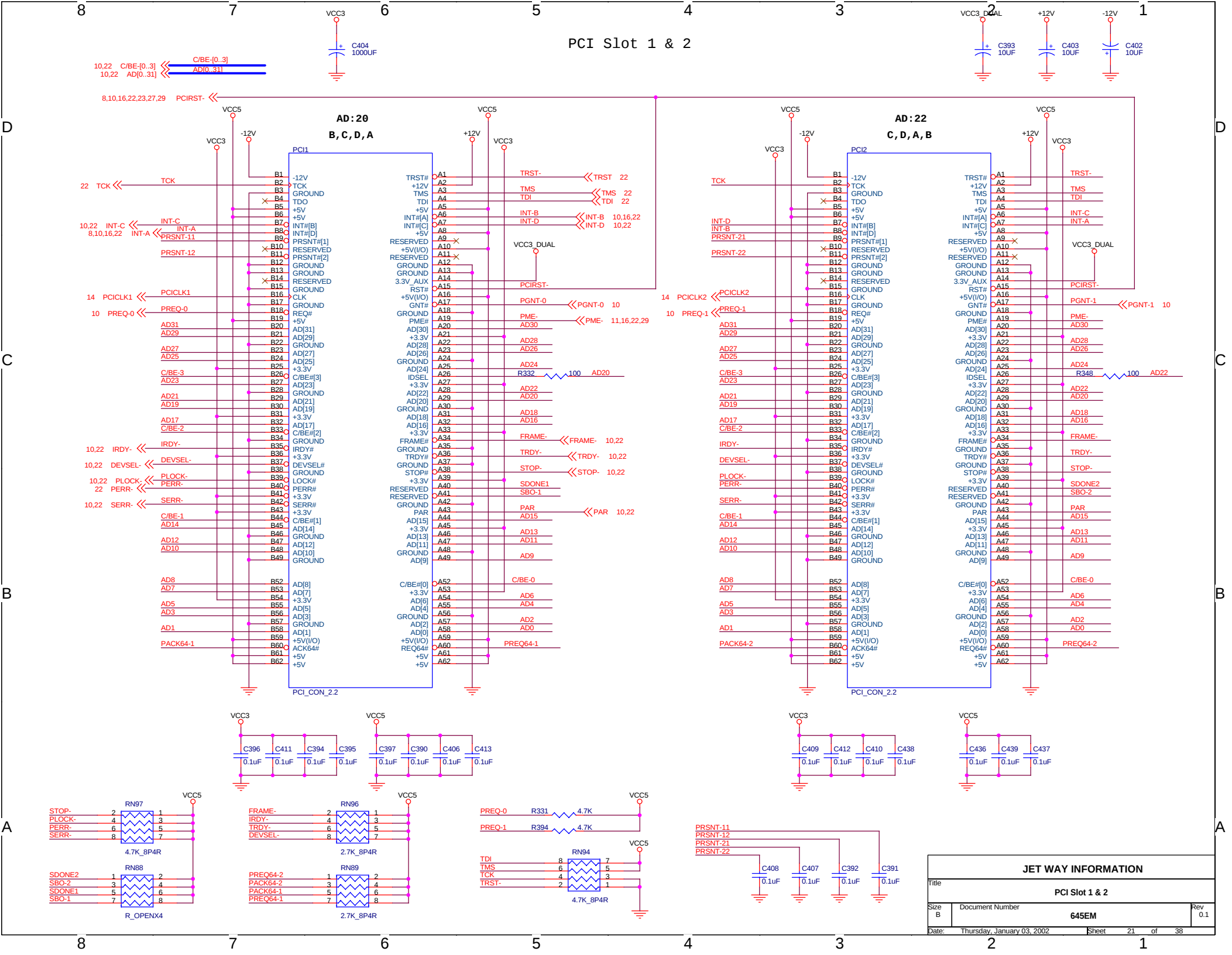
Title			
VGA Connector			
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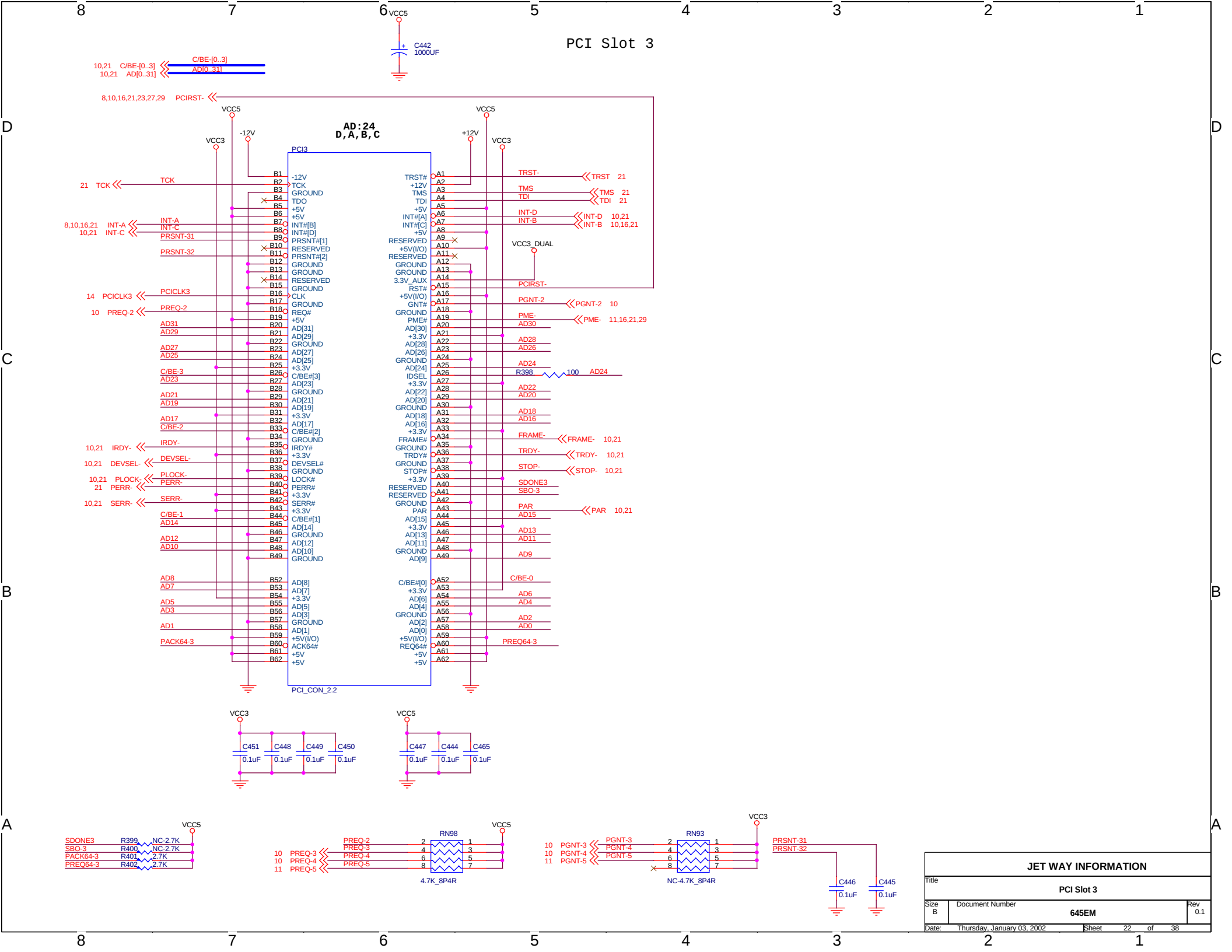


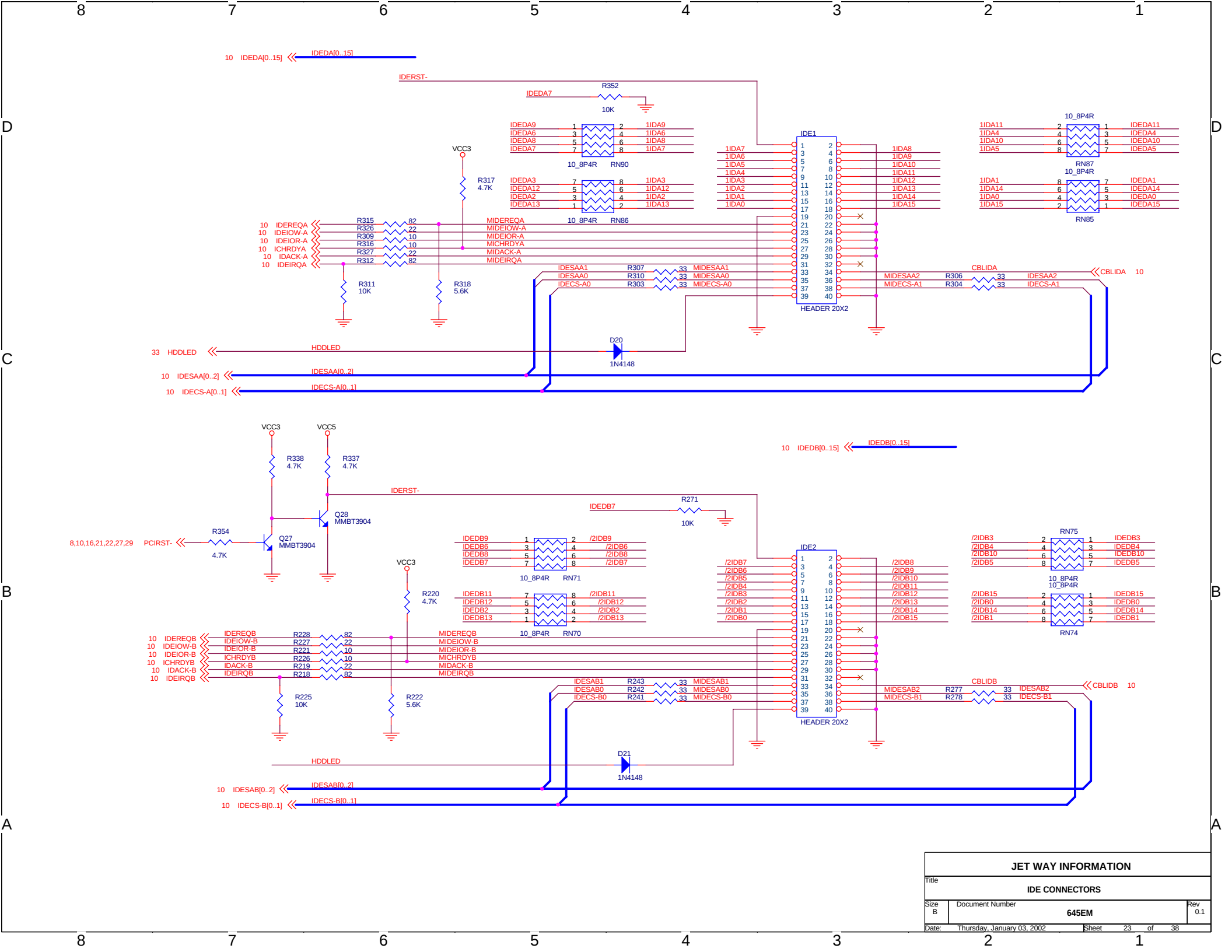




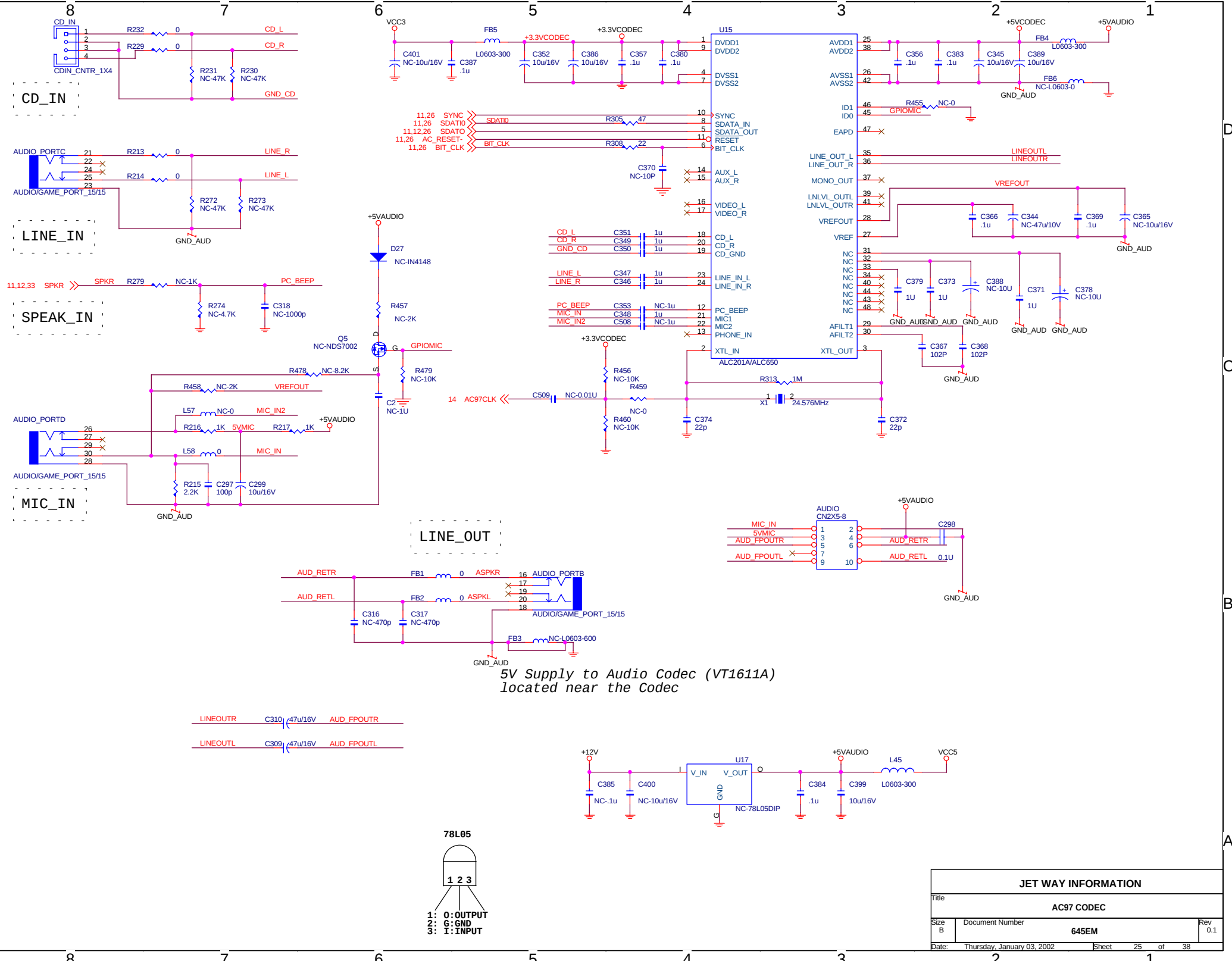
JET WAY INFORMATION			
Title		RESERVED	
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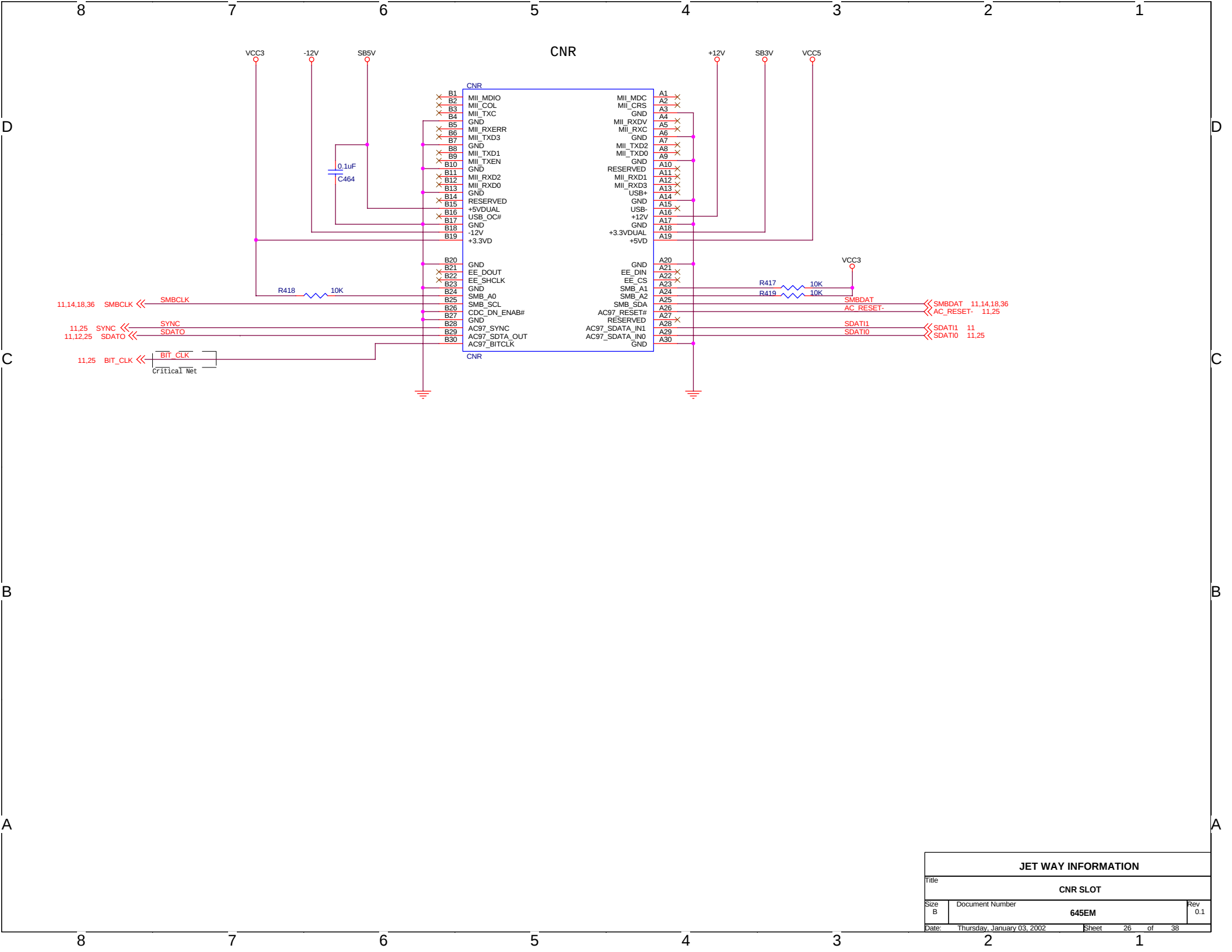




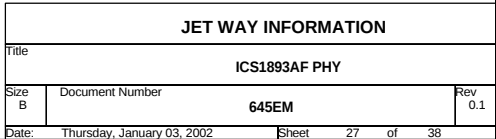


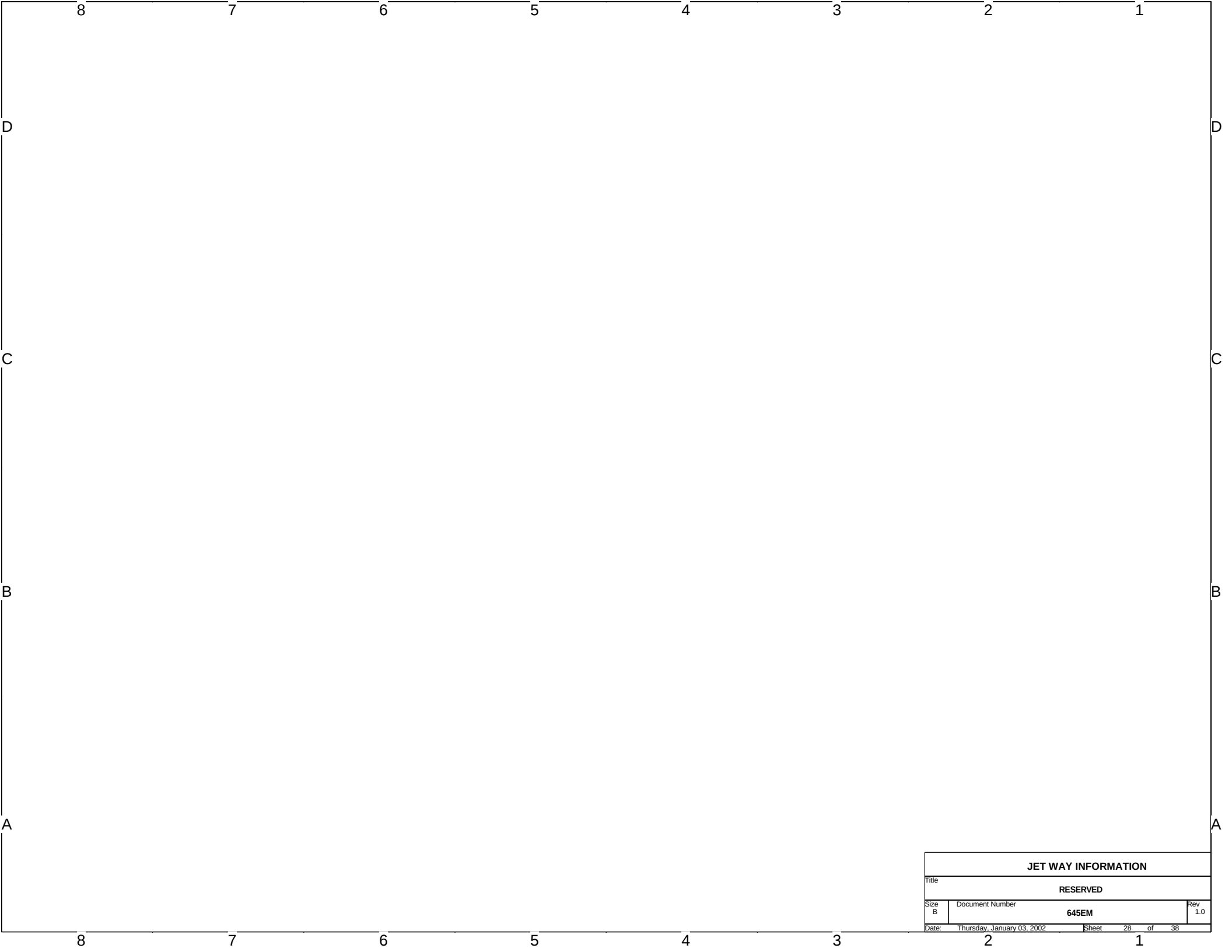
JET WAY INFORMATION			
Title			
IDE CONNECTORS			
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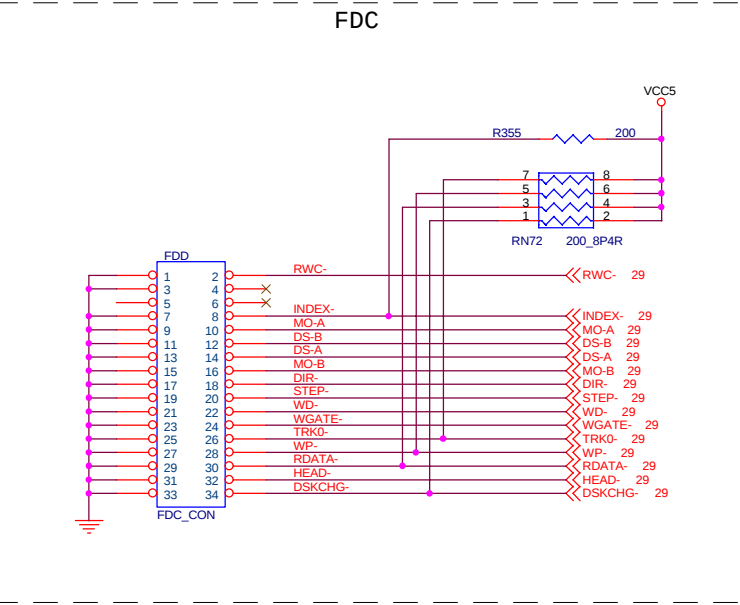
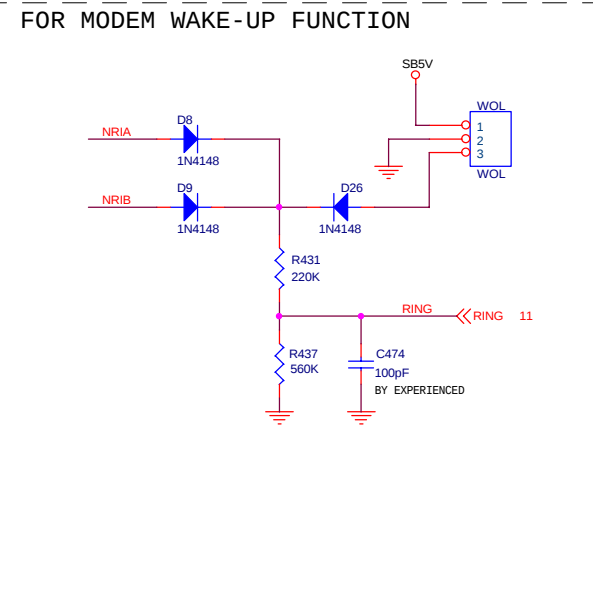
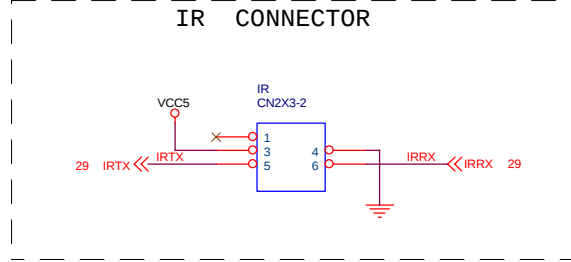
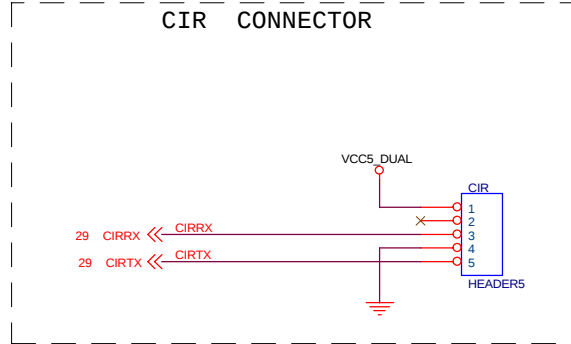
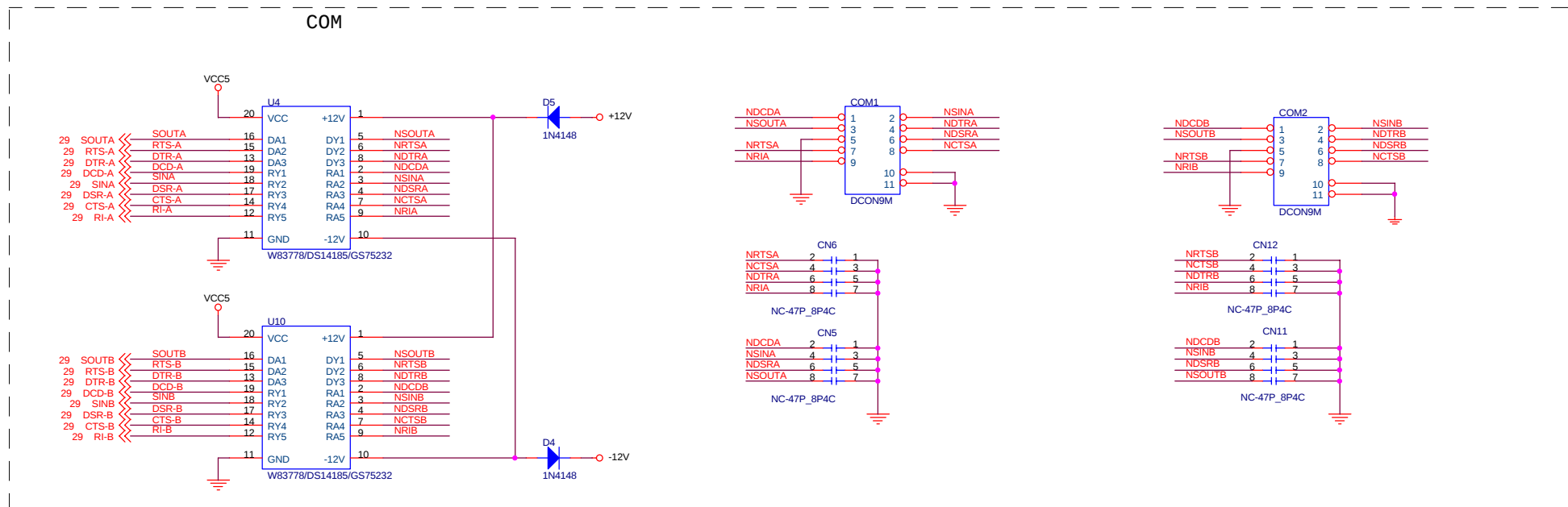


JET WAY INFORMATION			
Title		CNR SLOT	
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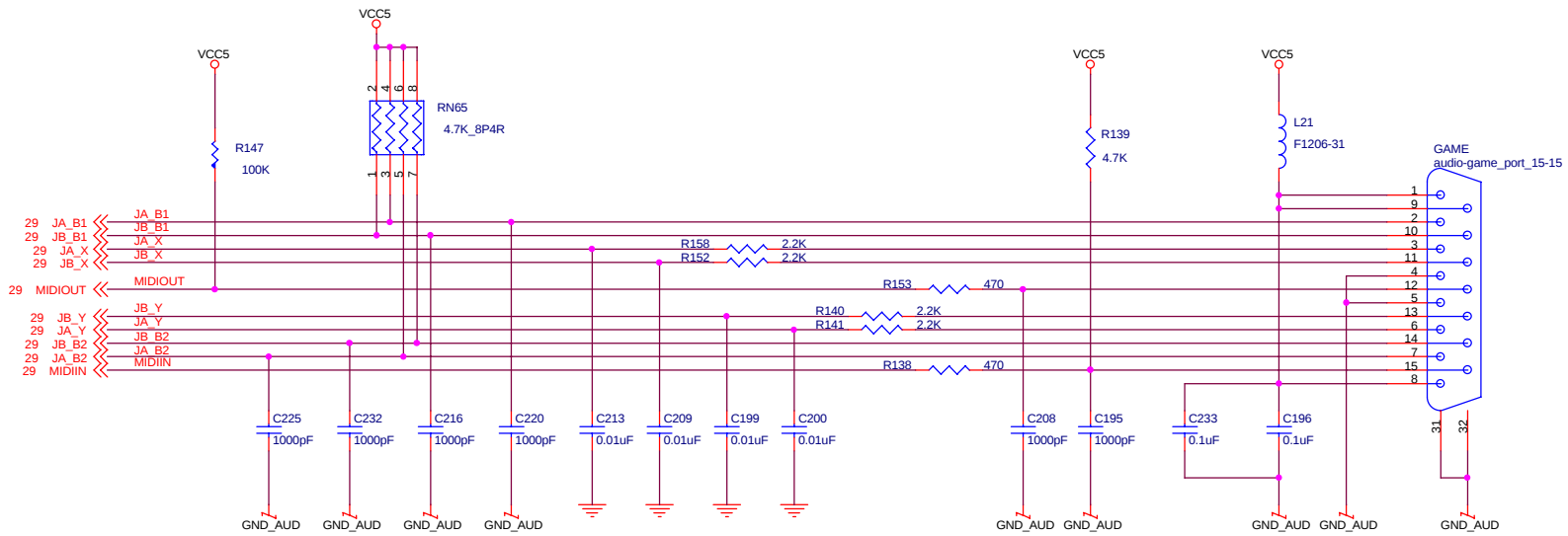


JET WAY INFORMATION			
Title		RESERVED	
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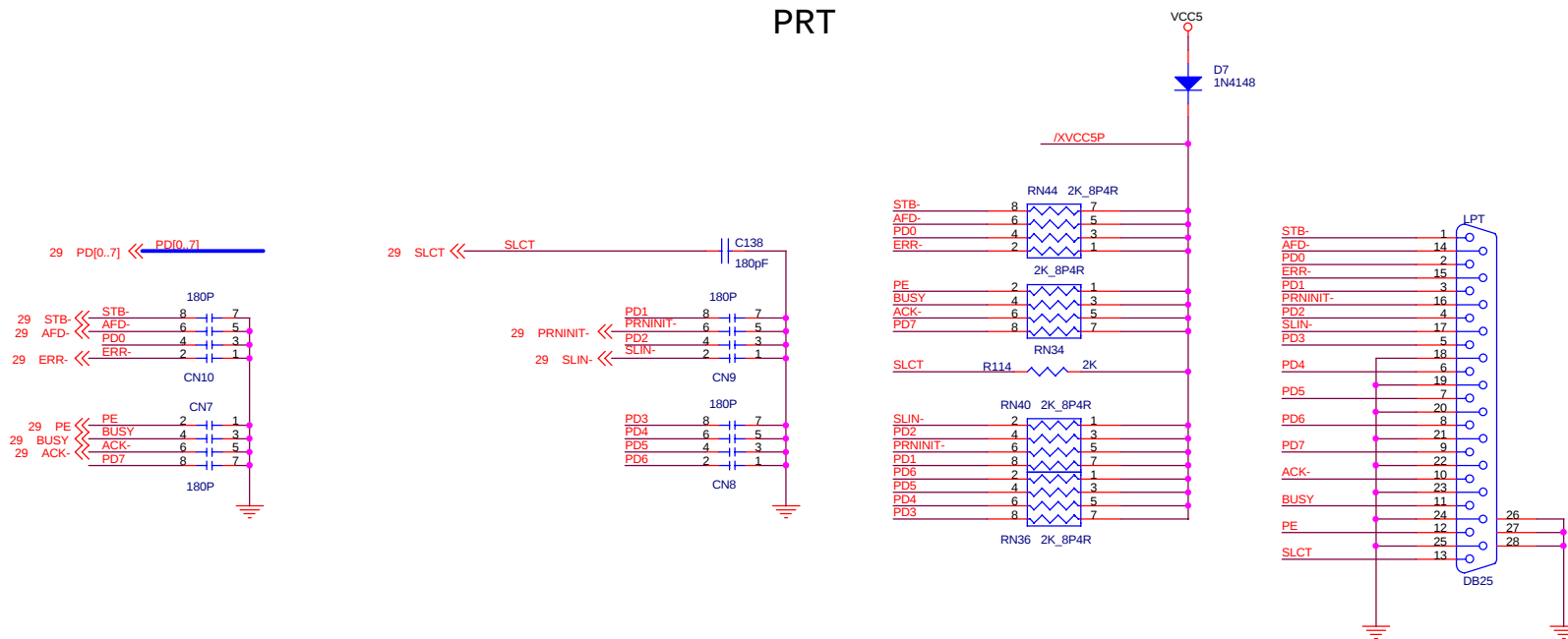


JET WAY INFORMATION			
Title			
FDC/COM1&2/IR CONN.			
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GAME PORT & MIDI



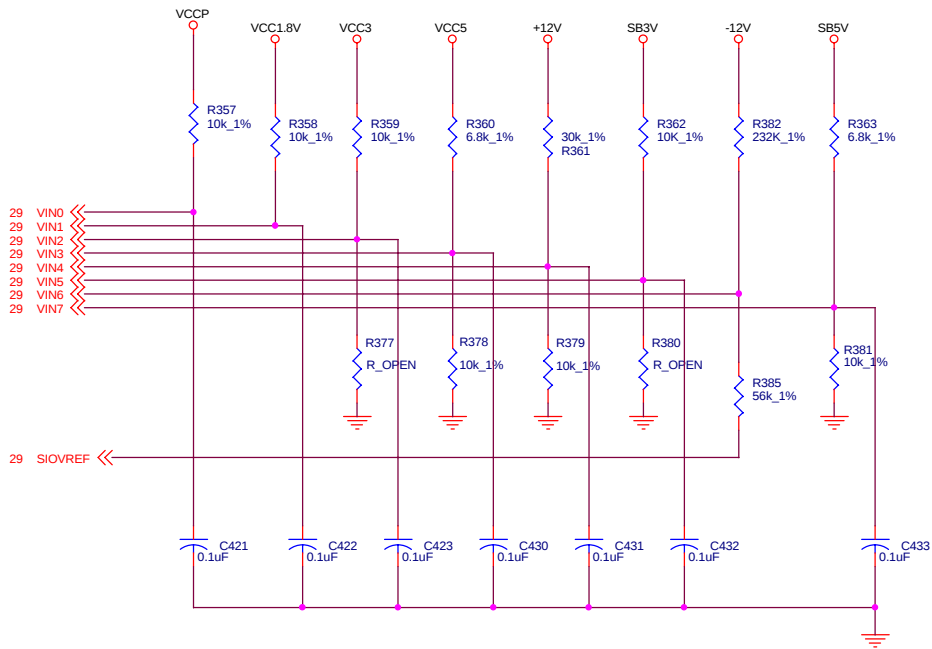
PRT



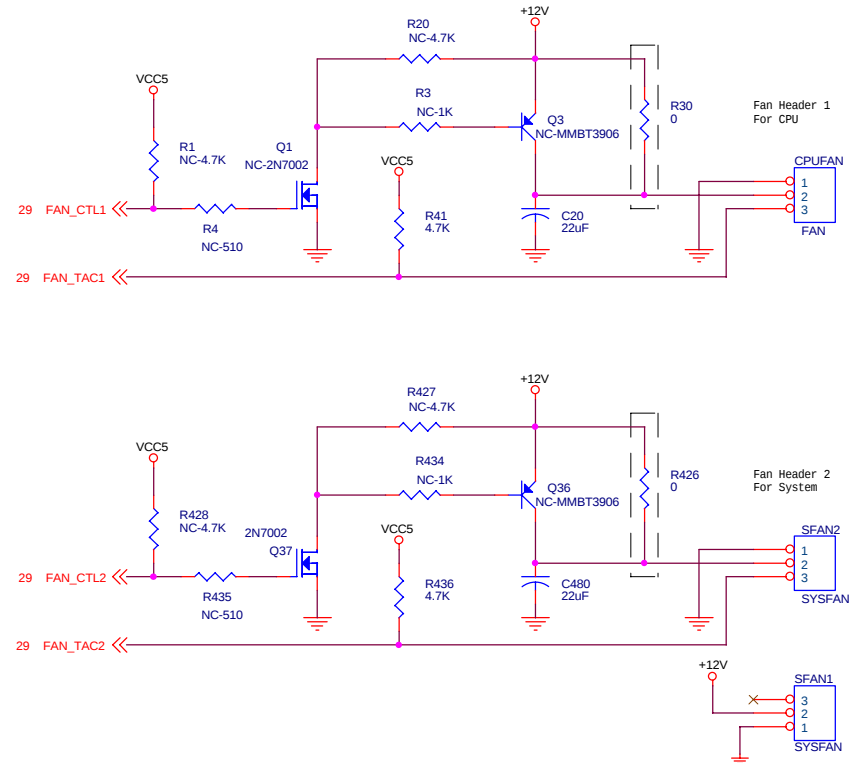
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Title			
GAME/PARALLEL CONN.			
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Voltage Monitor

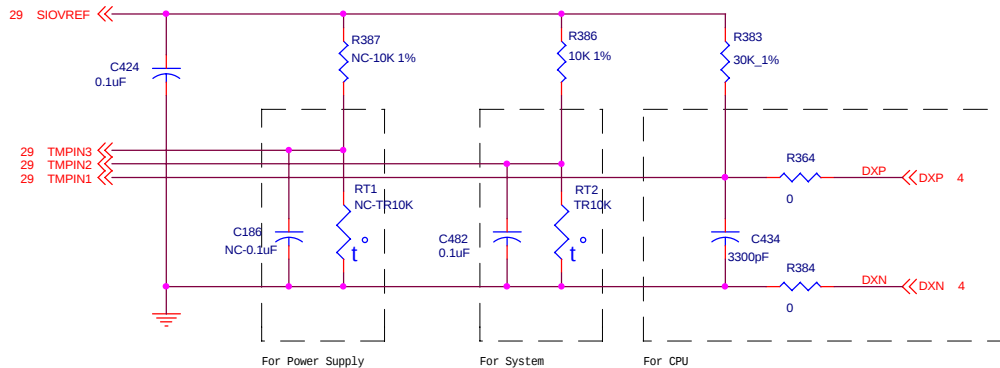


FAN Input and Output



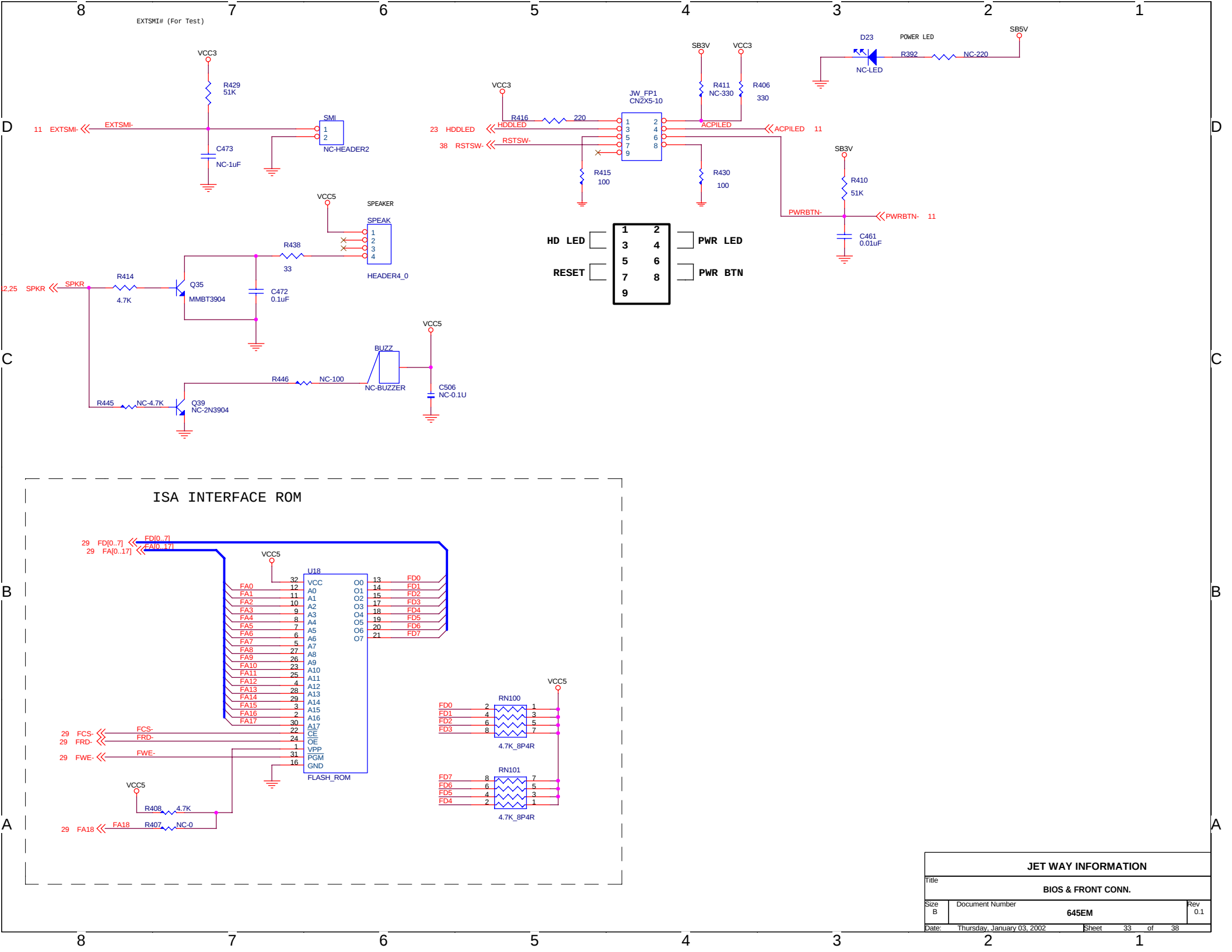
Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode



JET WAY INFORMATION

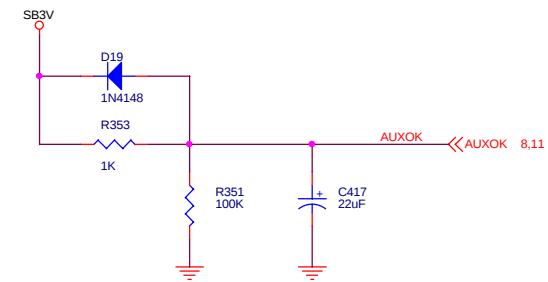
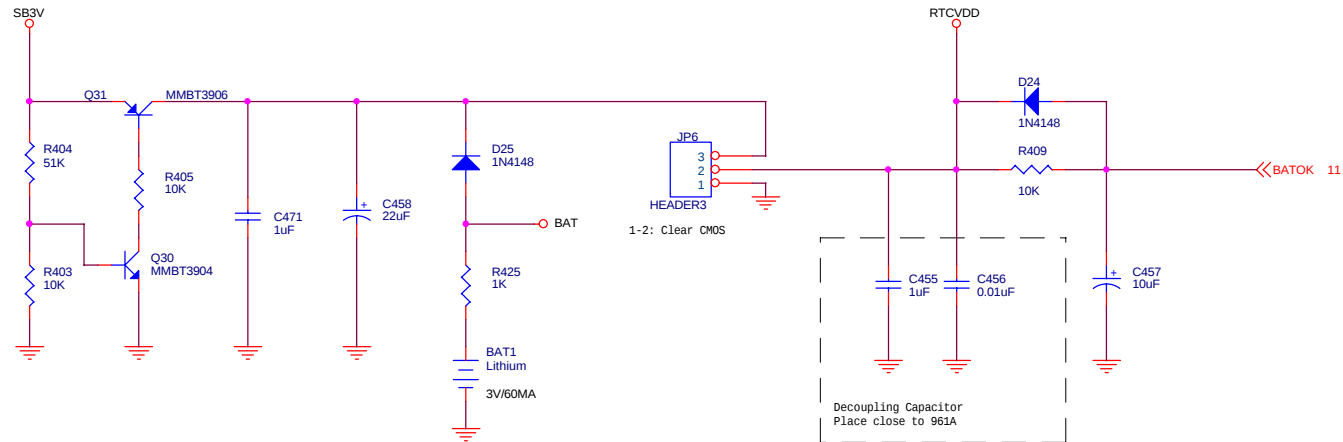
Title			
FAN1&2/VOLTAGE/TEMP			
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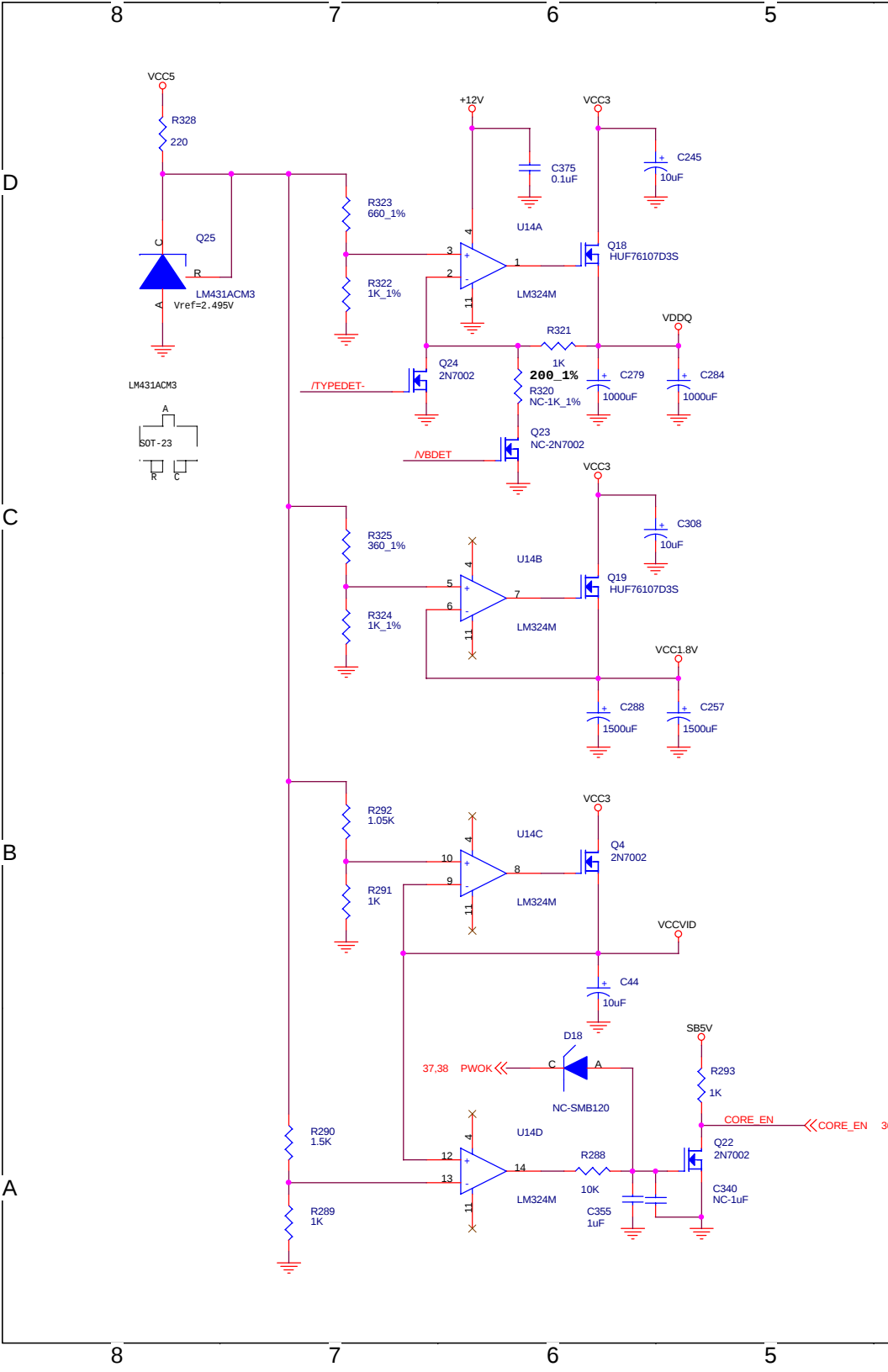
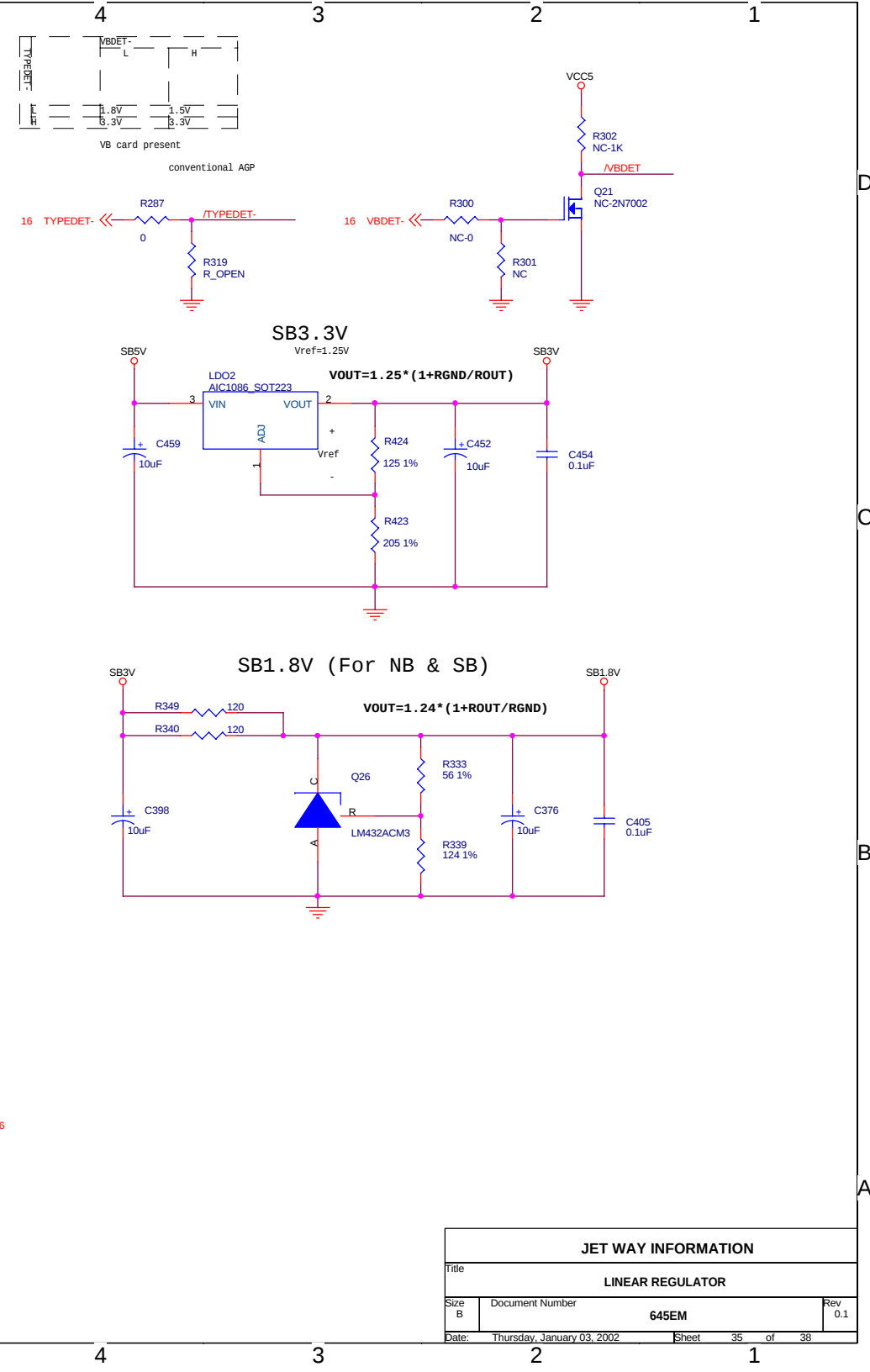
RTC

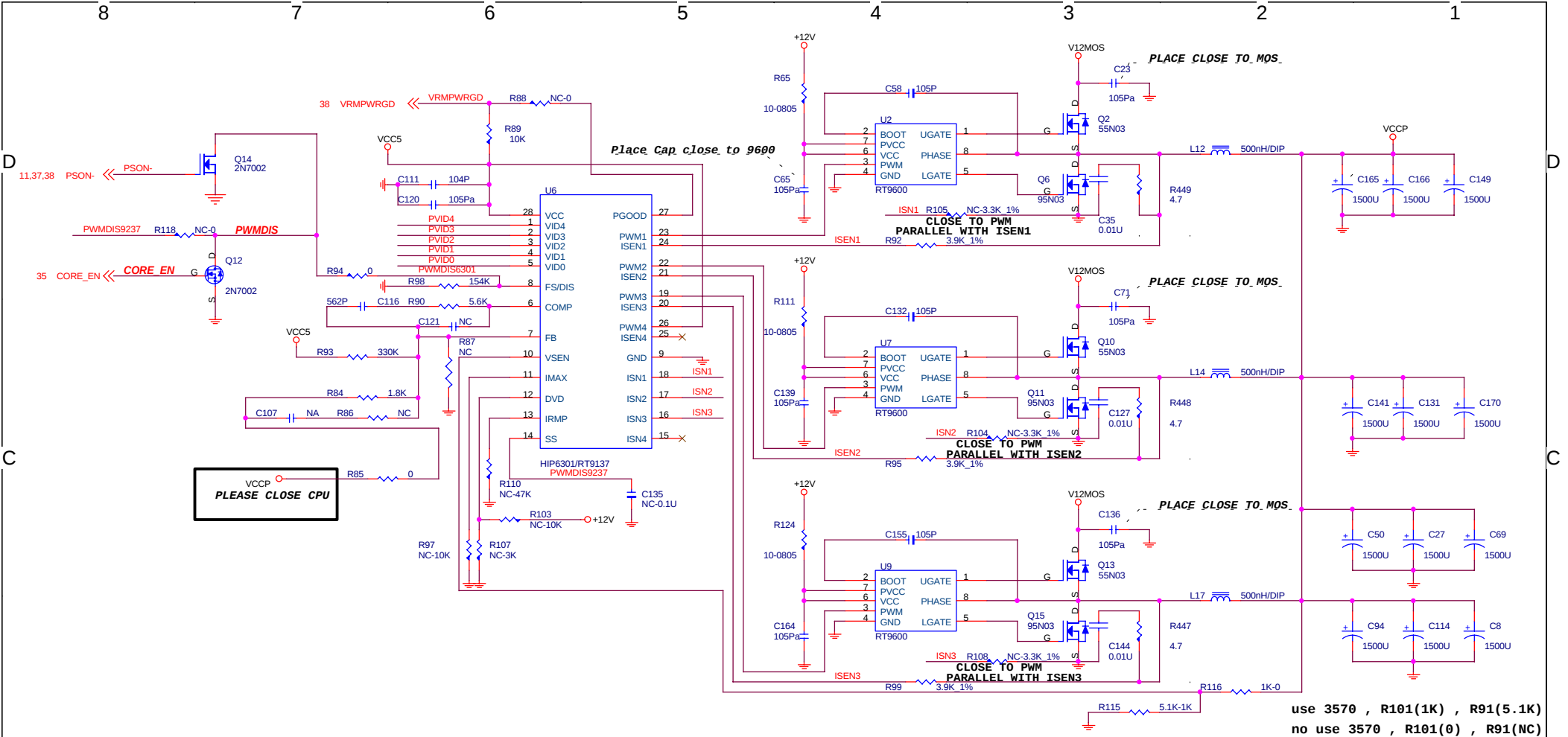
NOTE!

- 1.The RTCVDD is 3V
- 2.Decoupling capacitor must be close to 650 RTCVDD pin.
- 3.RTC circuit must strictly follow SiS's recommended design
SiS is not responsible for RTC problems from foreign designs.

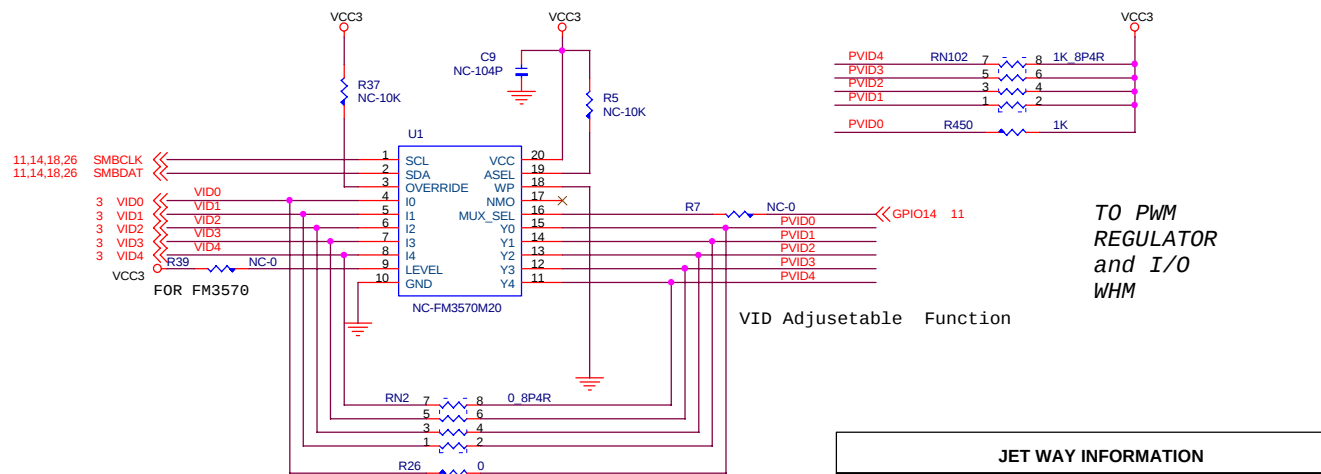


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Title		RTC	
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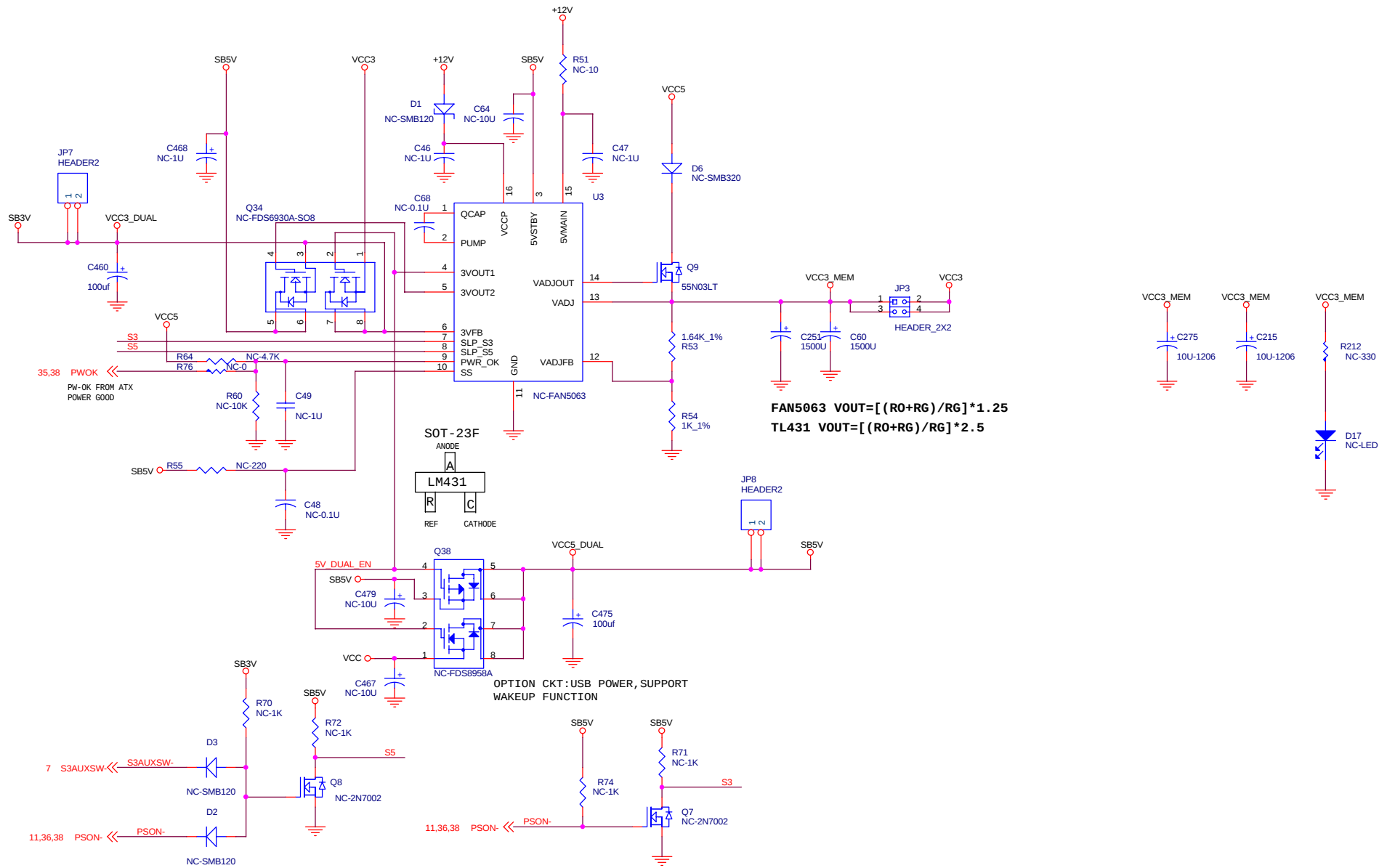




V1D4	V1D3	V1B2	V1D1	V1D0	VCORE
1	1	1	1	0	1.100
1	1	1	1	1	1.125
1	1	1	0	0	1.150
1	1	1	0	1	1.175
1	1	0	0	1	1.200
1	1	0	1	0	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	0	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

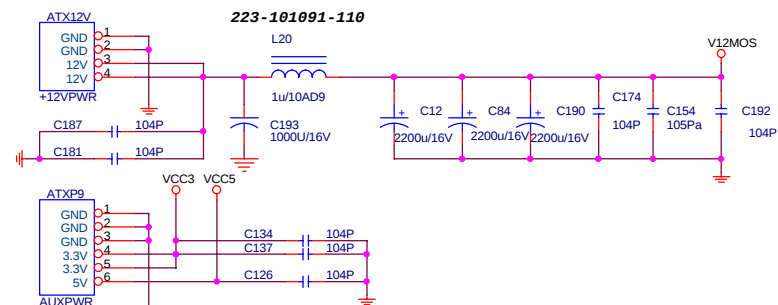
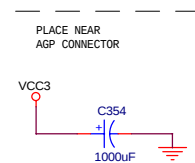
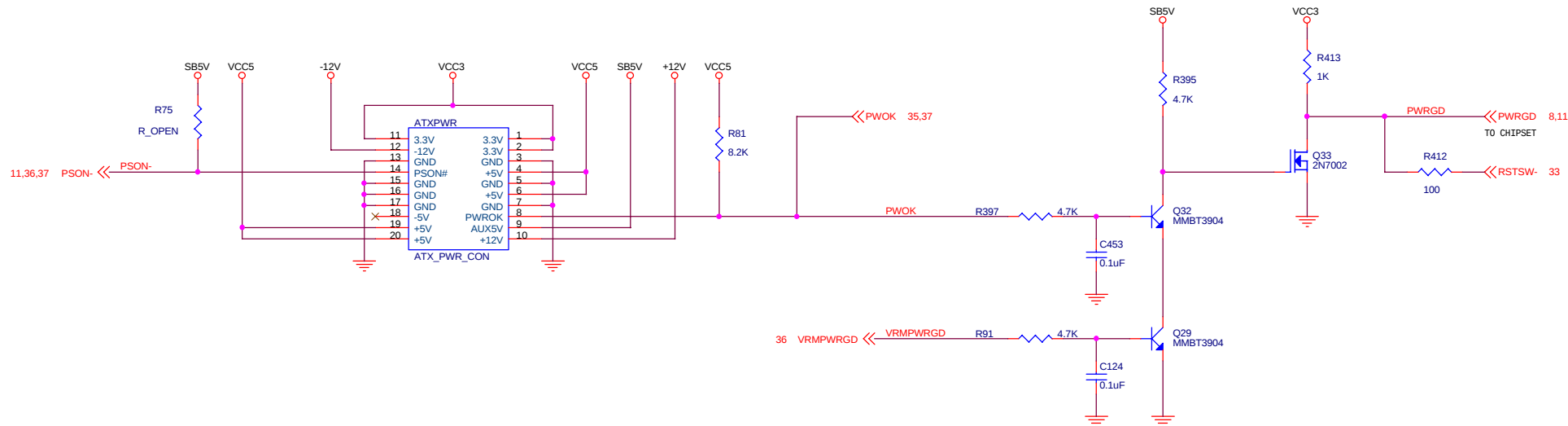


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CPU POWER									
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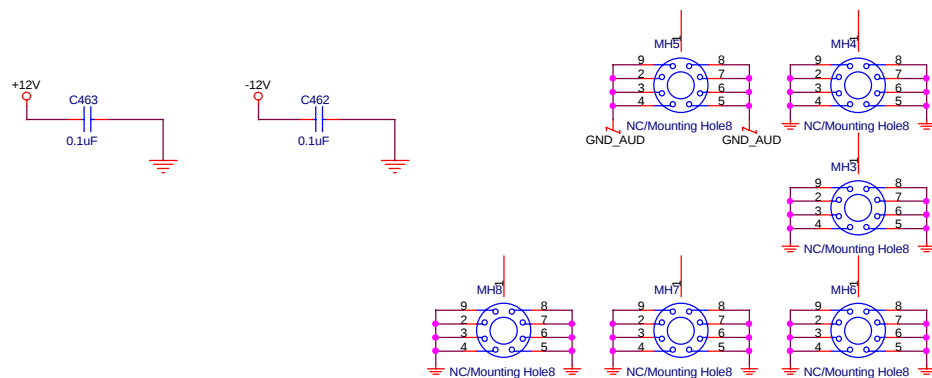


MODE	CONTROL	SIGNAL			
	PSN#	S3AUXSW-	S3	S5	
S0->S3	0	0	1	1	1
S0	0	1	1	1	1
S3	1	0	0	1	1
S5	1	1	0	0	0

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ACPI POWER			
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