

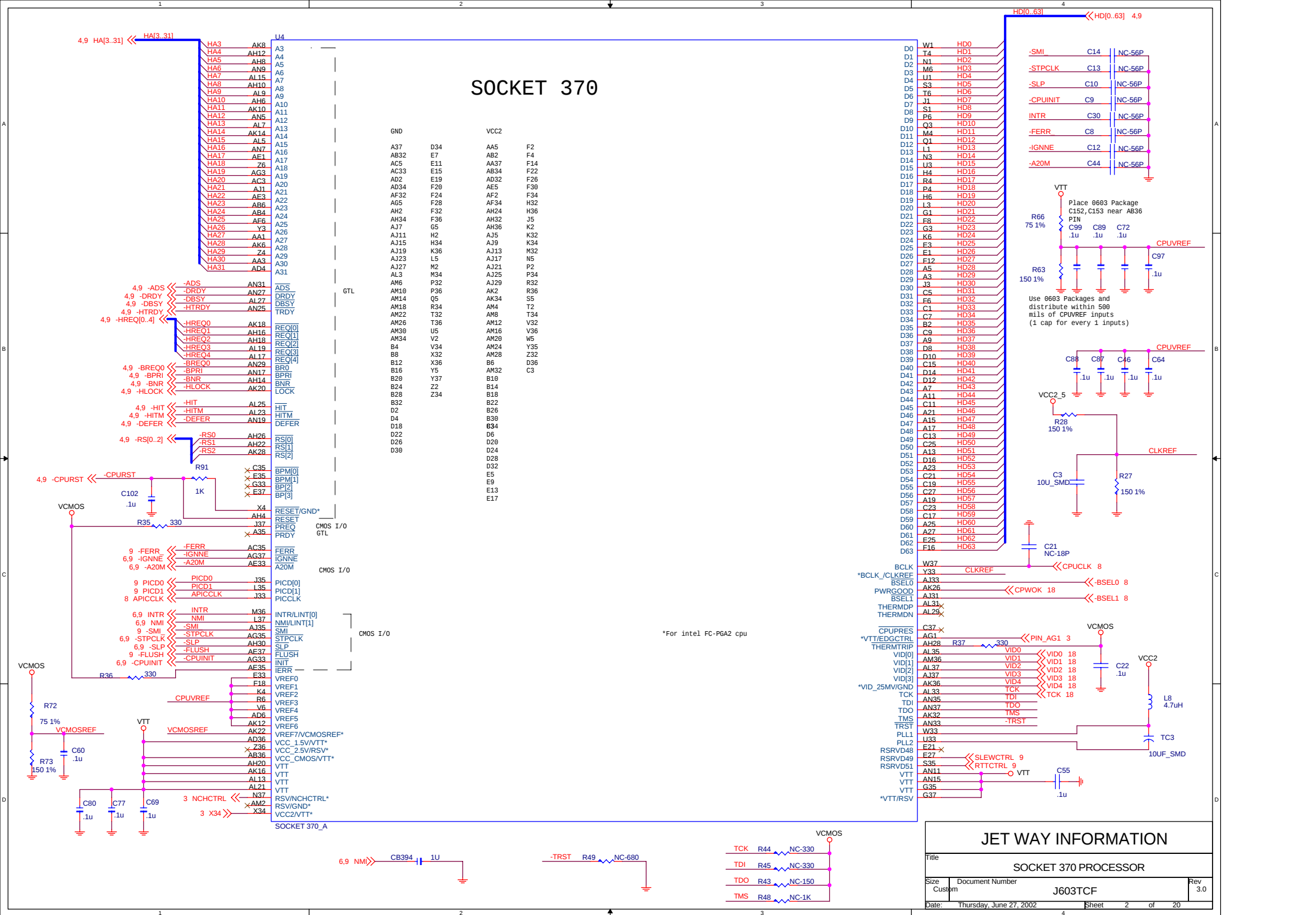
VIA Apollo ProMedia Board Schematics

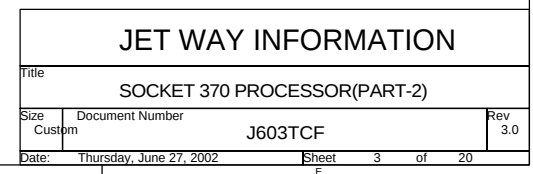
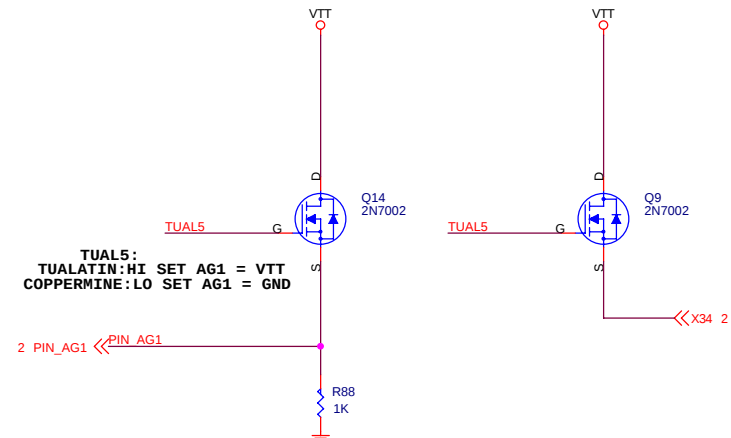
603TCF

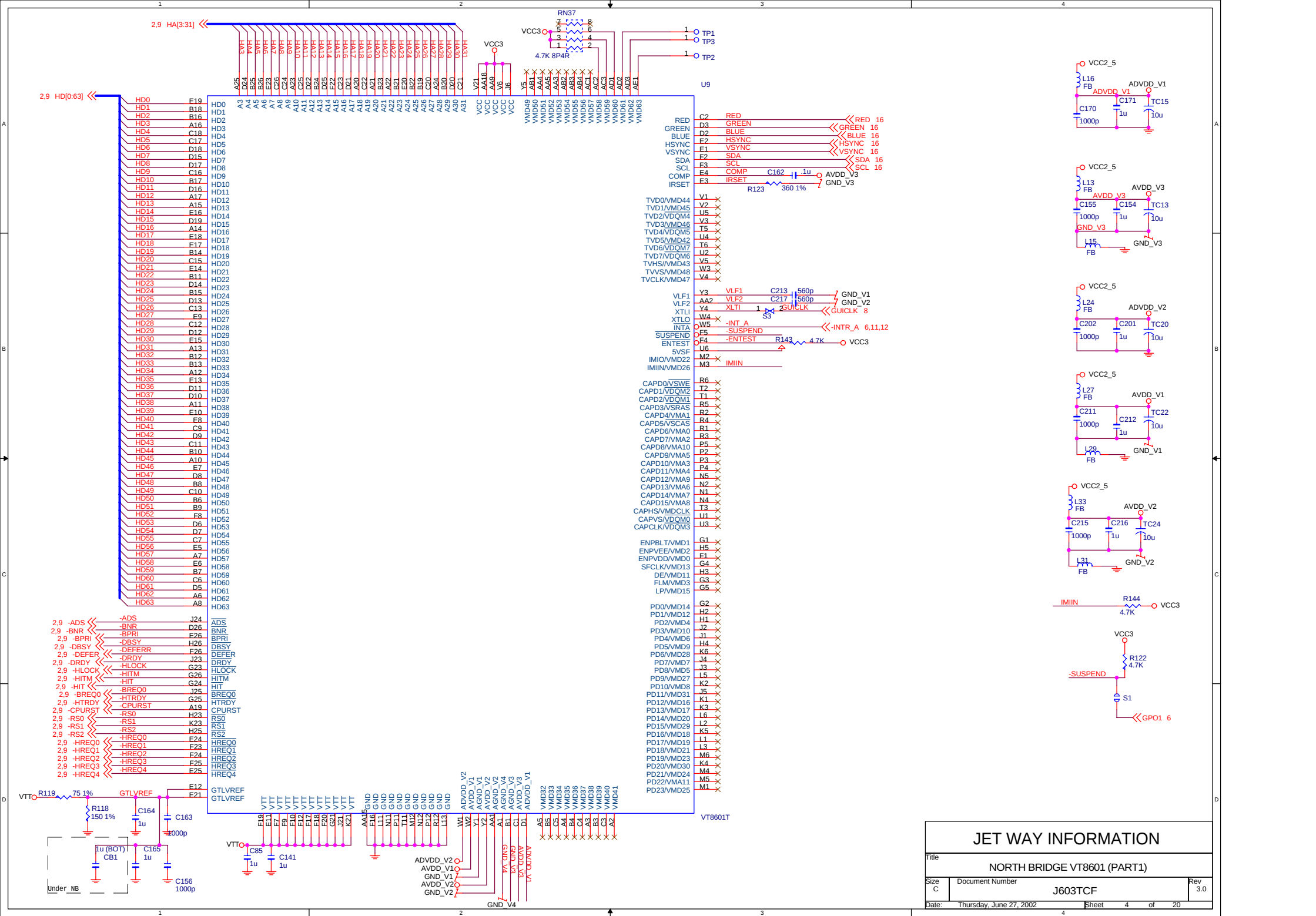
TITLE	SHEET No.
COVER SHEET	1
SOCKET 370 PROCESSOR	2, 3
NORTH BRIDGE VT8601/A	4, 5
SOUTH BRIDGE VT82C686A/B	6, 7
CLOCK SYNTHESIZER	8
AGTL+ BUS AND PULL UP RESISTORS	9
SDRAM DIMM SLOTS 1/2	10
PCI SLOT1 & PCI SLOT2	11
PCI SLOT3 & USB 2/3	12
ISA SLOT & SYSTEM ROM	13
IDE CONNECTORS & WAKE UP CIRCUITRY	14
FRONT PANEL & BACK PANEL CONNECTOR (USB 0/1)	15
FAN CONTROL CIRCUITRY & VGA CONNECTOR	16
AC'97 AUDIO CODEC & AUDIO PORTS	17
DC-DC CONVERTERS	18
ATX POWER CONNECTORS & BYPASS CAPACITORS	19
RTL 8100BL LAN	20

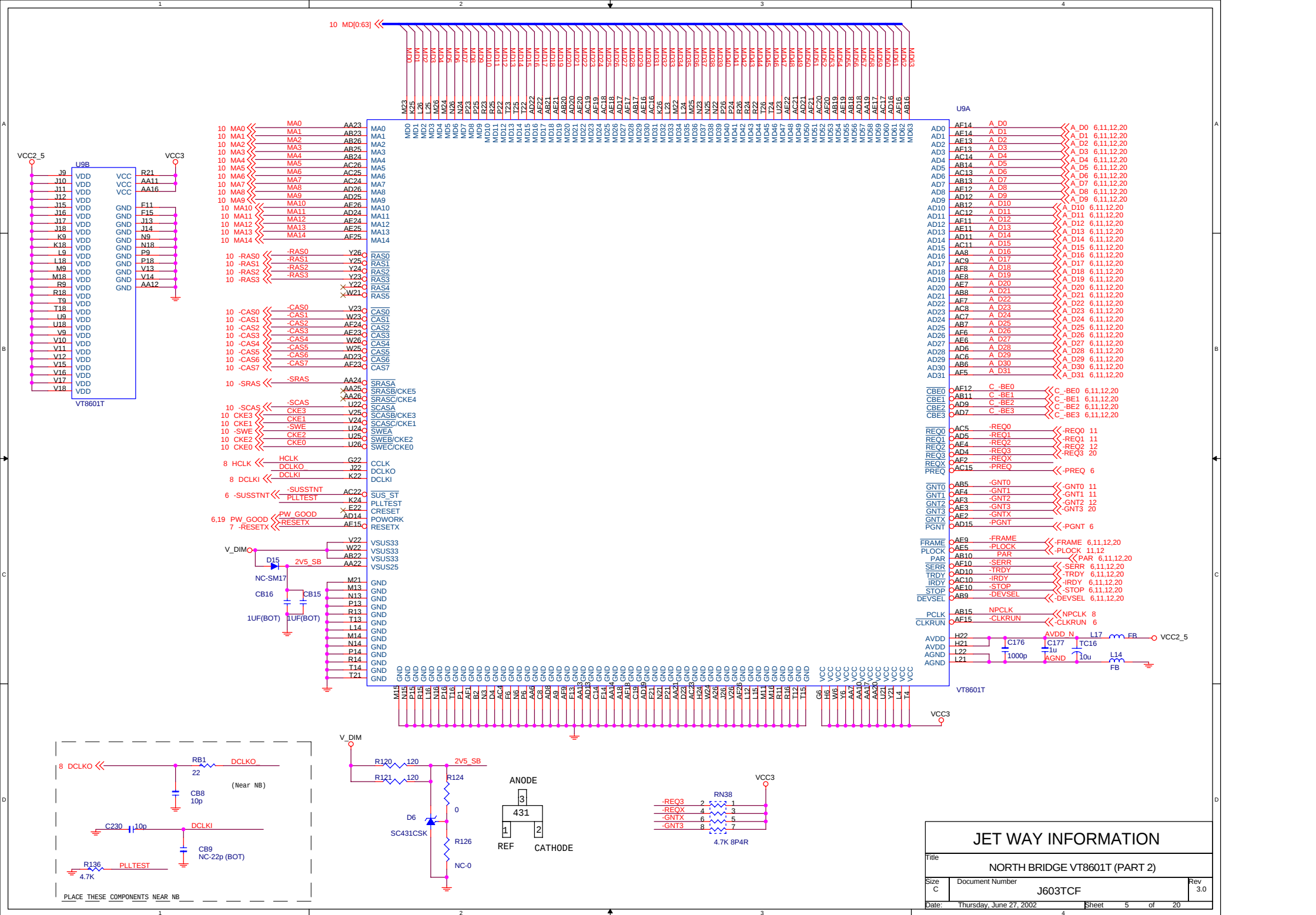
VIA TECHNOLOGIES ASSUMES NO RESPONSIBILITY FOR ANY ERRORS
IN DRAWING THESE SCHEMATICS. THESE SCHEMATICS ARE SUBJECT
TO CHANGE AT ANY TIME WITHOUT NOTICE.
COPYRIGHT 2000 VIA TECHNOLOGIES INCORPORATED.

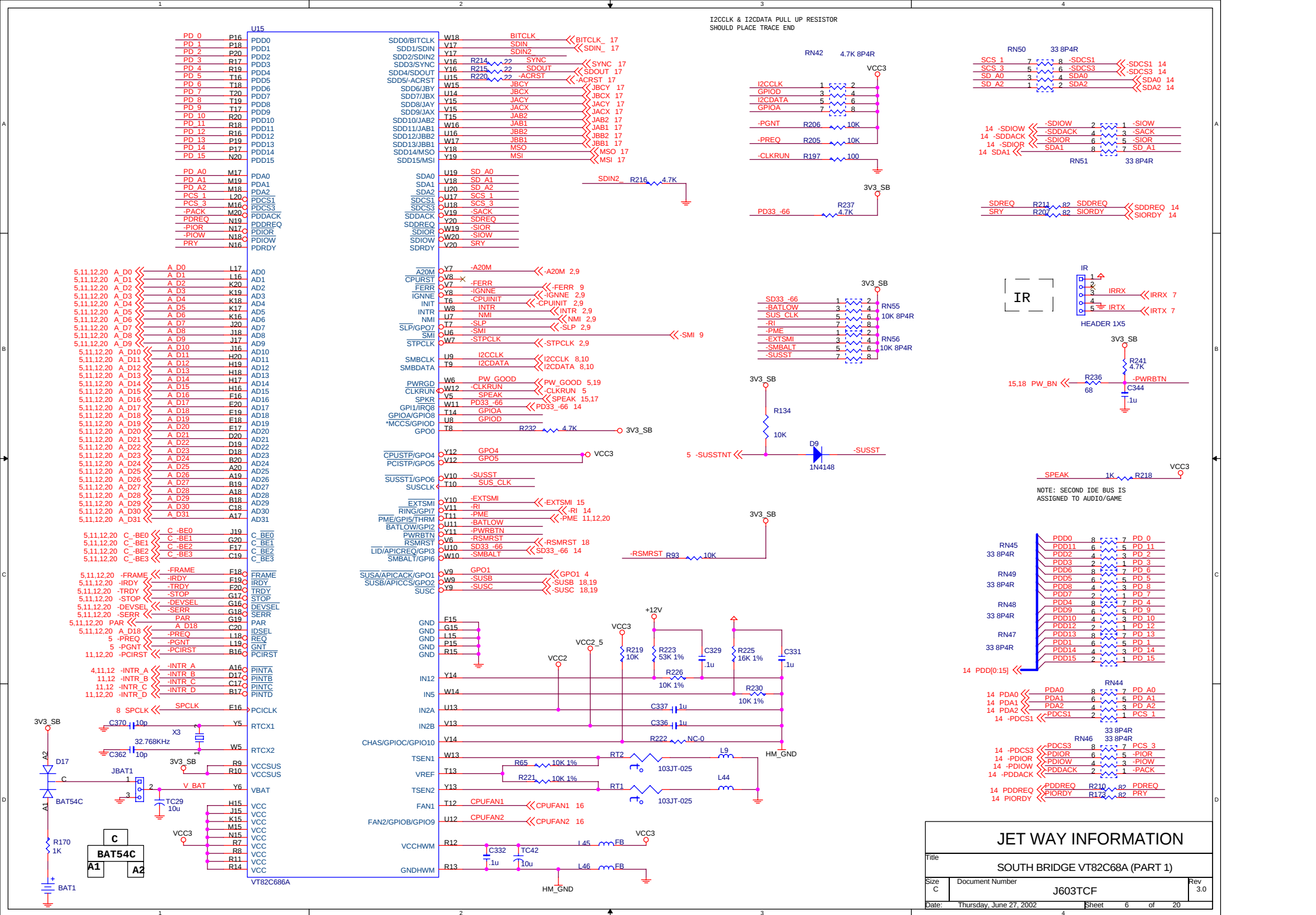
JET WAY INFORMATION			
Title COVER SHEET			
Size Custom	Document Number J603TCF		Rev 3.0
Date: Thursday, June 27, 2002	Sheet 1 of 20		

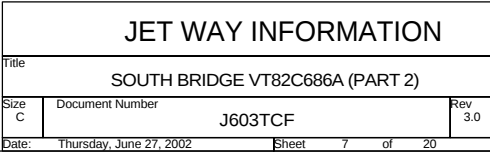


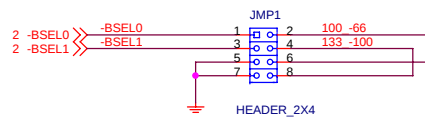
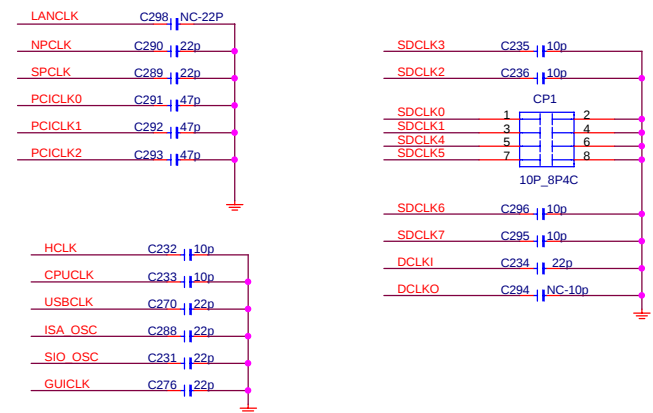




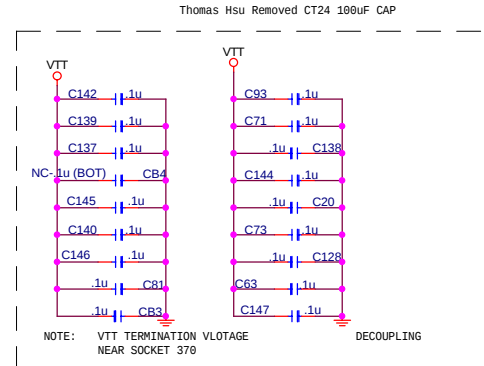
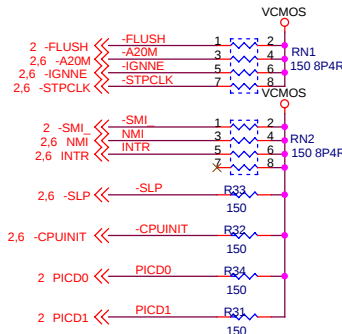
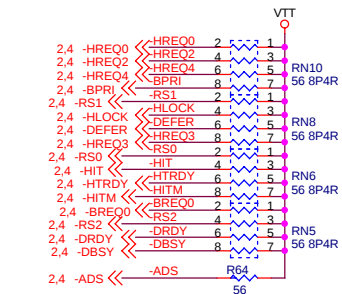
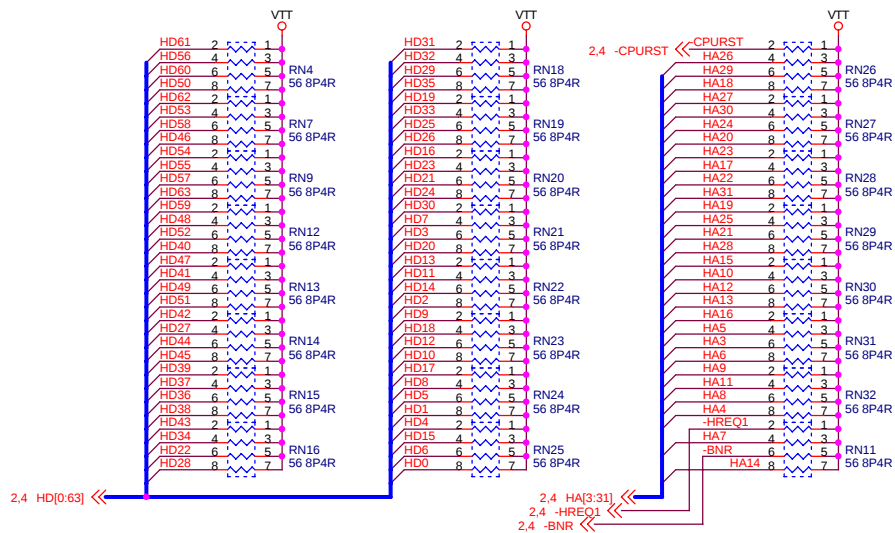
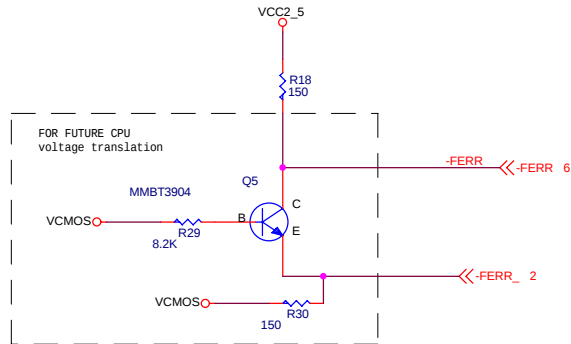




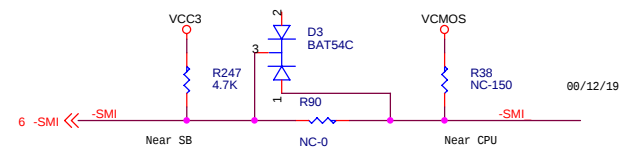




JET WAY INFORMATION			
Title			
CLOCK SYNTHESIZER			
Size C	Document Number J603TCF		Rev 3.0
Date:	Thursday, June 27, 2002	Sheet	8 of 20

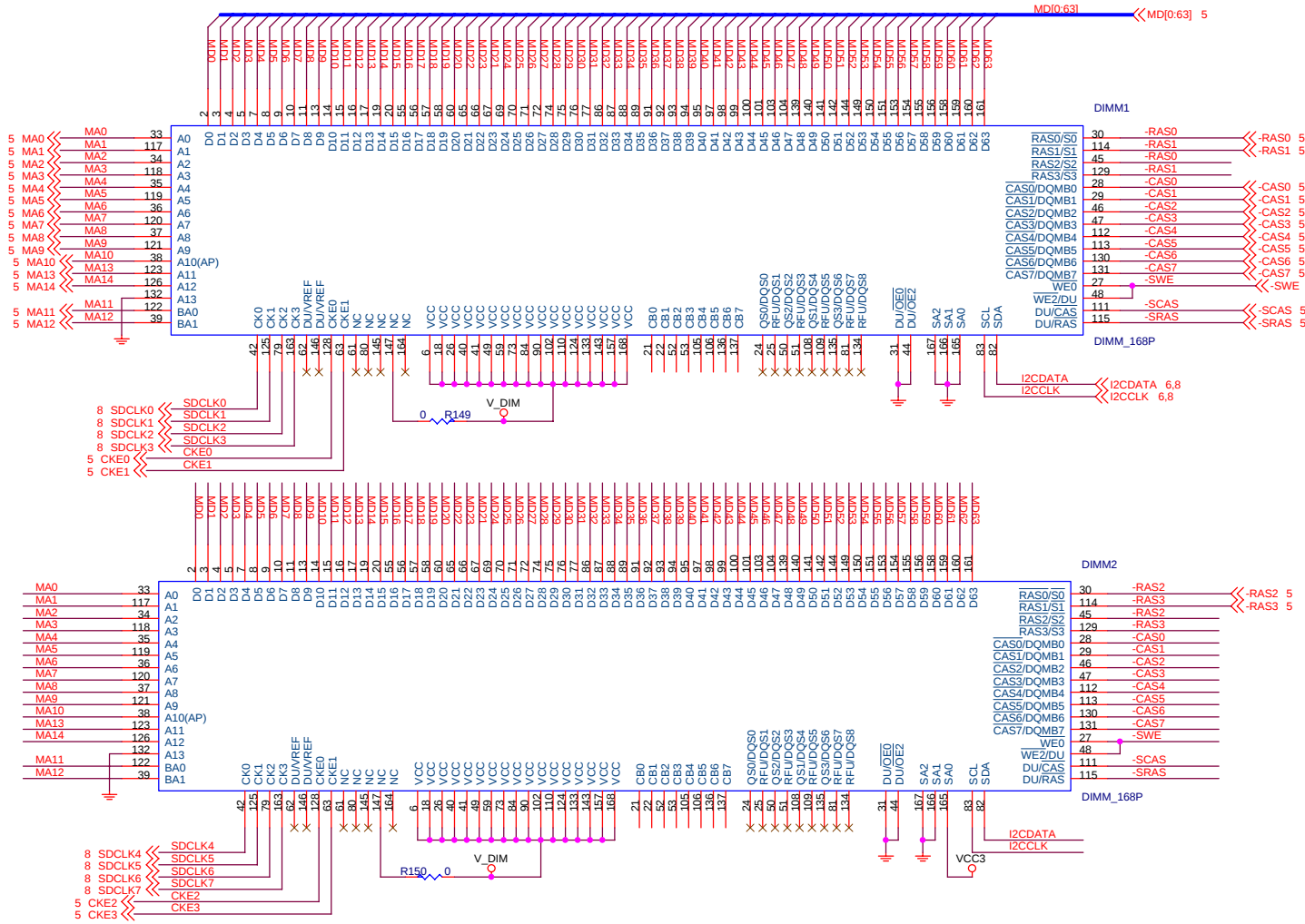


Thomas modified for detecting Ratio by CPU

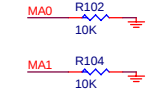
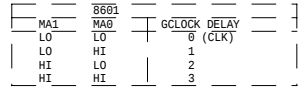


JET WAY INFORMATION

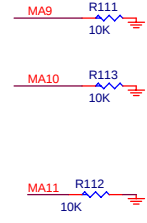
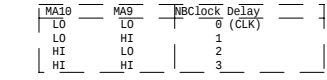
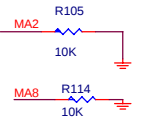
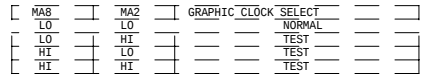
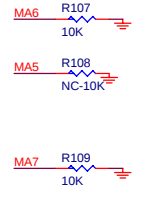
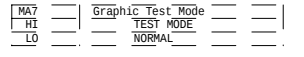
Title		
AGTL+ PULL UP RESISTORS		
Size C	Document Number	Rev
	J603TCF	3.0
Date:	Thursday, June 27, 2002	Sheet 9 of 20



MA POWER-UP STRAPPING OPTIONS

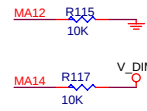


MA6:LO DISABLE LCD FUNCTION



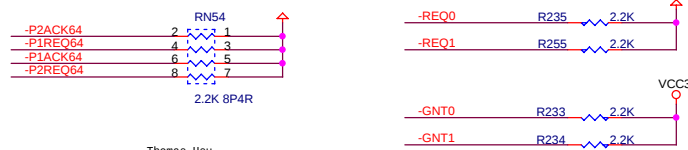
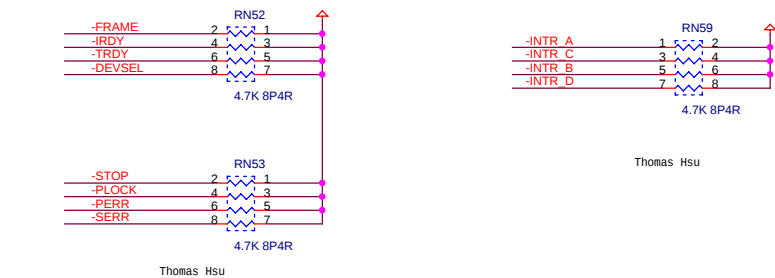
CPU FREQ FIX AUTO MODE

Thomas



JET WAY INFORMATION

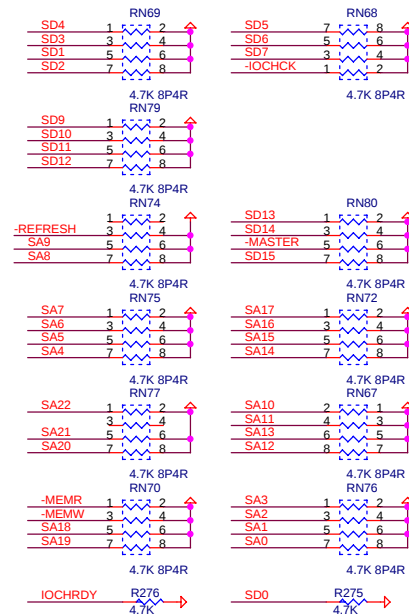
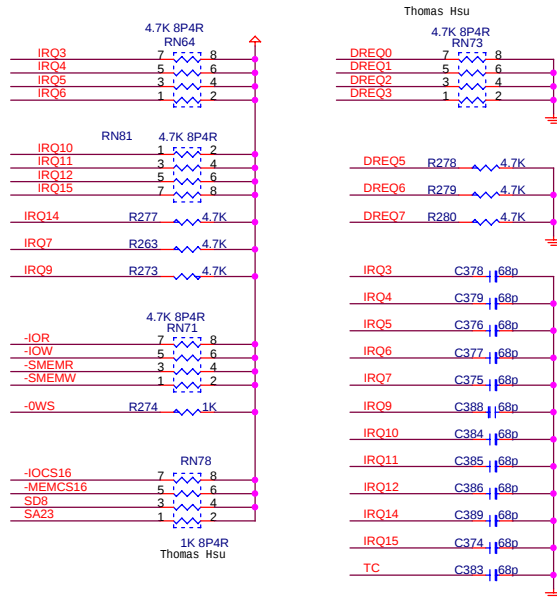
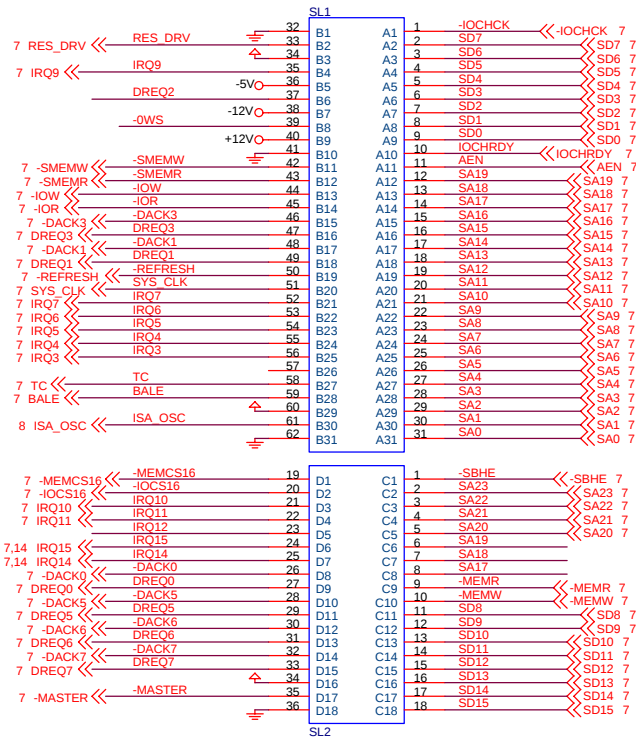
Title			SDRAM DIMM SLOTS	
Size	Document Number	J603TCF		Rev
C				3.0
Date:	Thursday, June 27, 2002	Sheet	10 of 20	

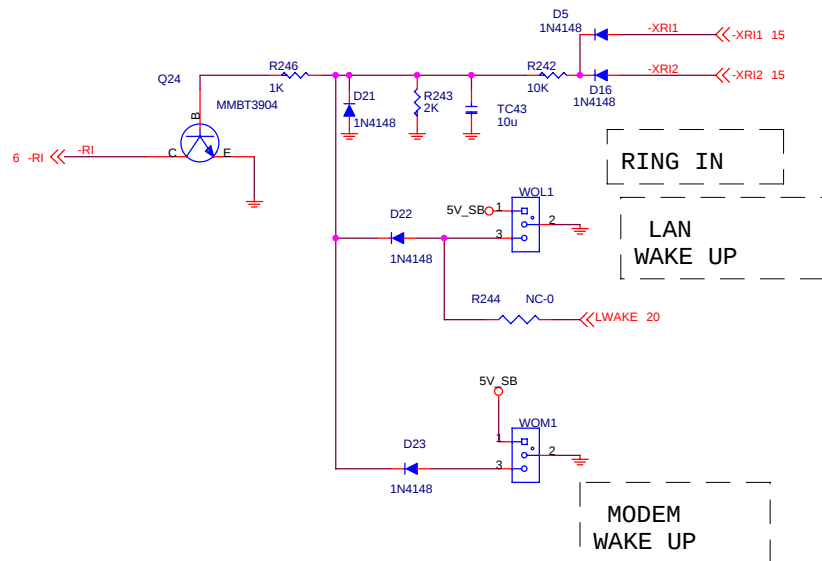


Title			
PCI1 & PCI2 SLOTS			
Size	Document Number		Rev
C	J603TCF		3.0
Date:	Thursday, June 27, 2002	Sheet	11 of 20

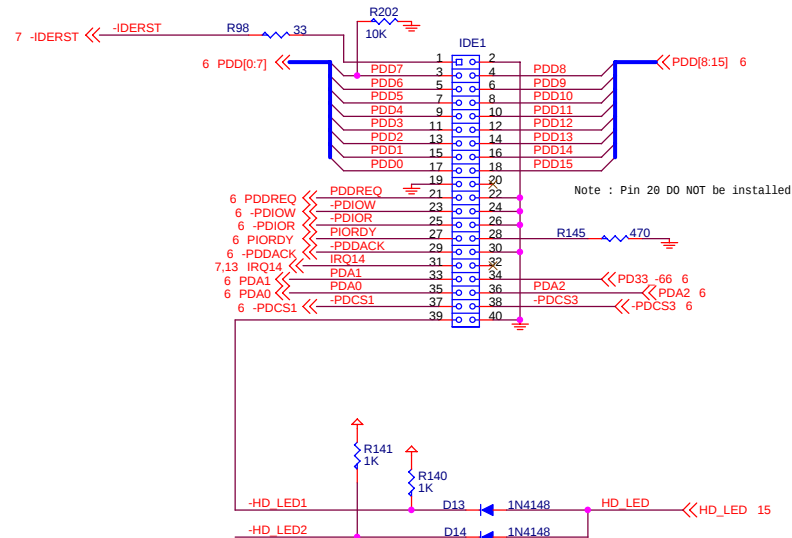


JET WAY INFORMATION

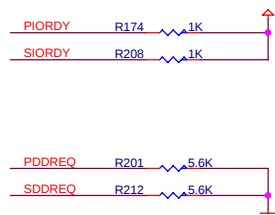
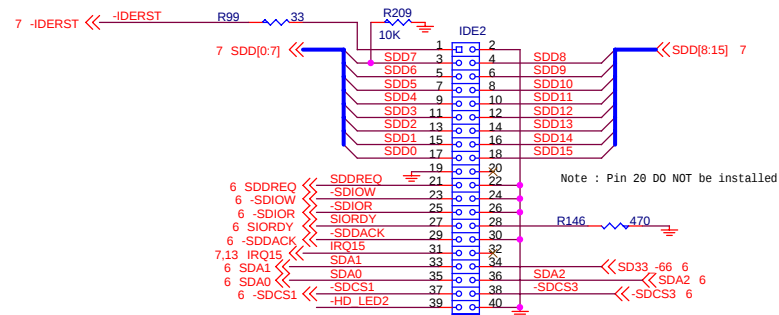




PRIMARY



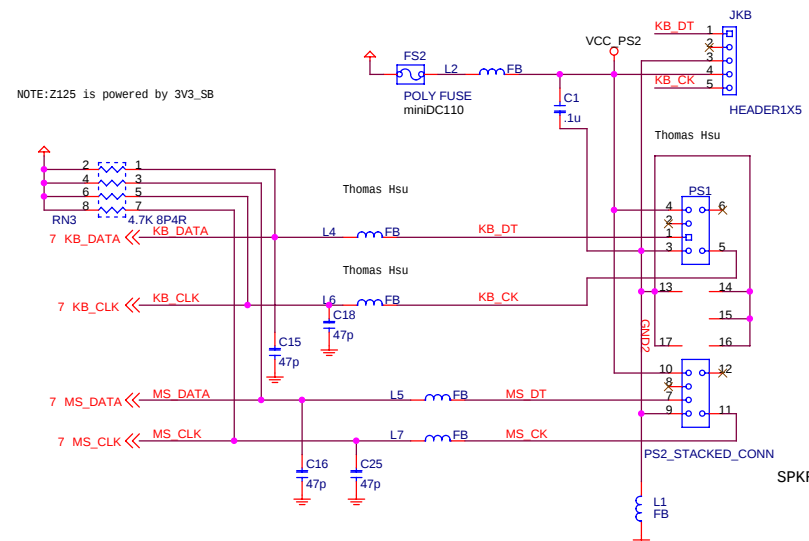
SECONDARY



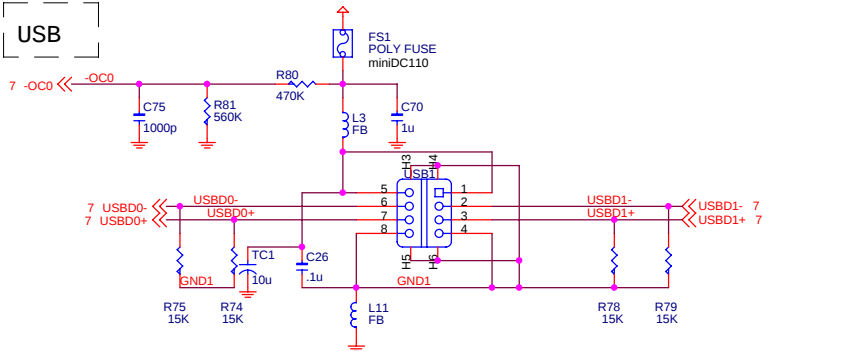
JET WAY INFORMATION

Title		
IDE1 & IDE2		
Size	Document Number	Rev
C	J603TCF	3.0
Date:	Thursday, June 27, 2002	Sheet 14 of 20

PS2

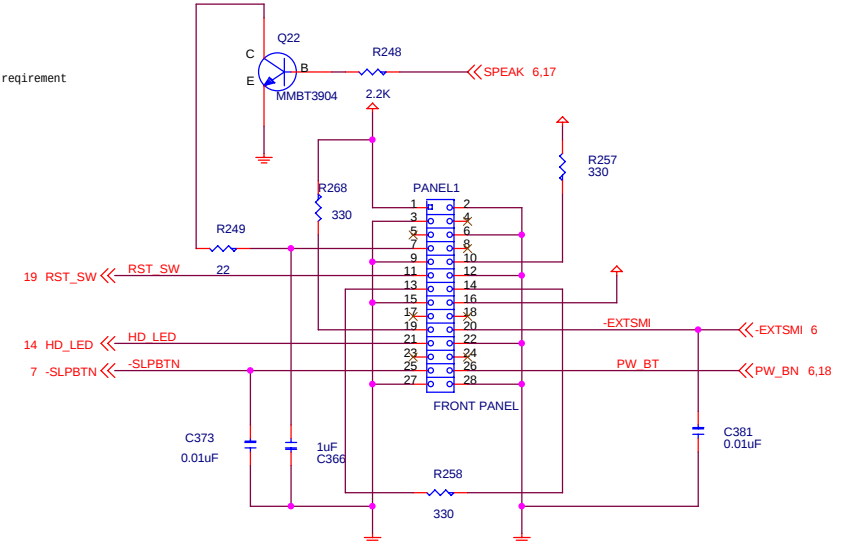
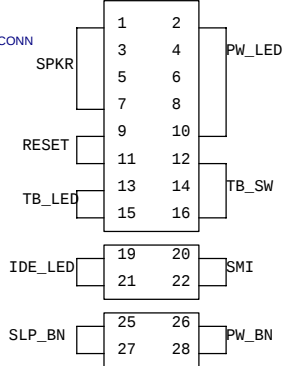


USB

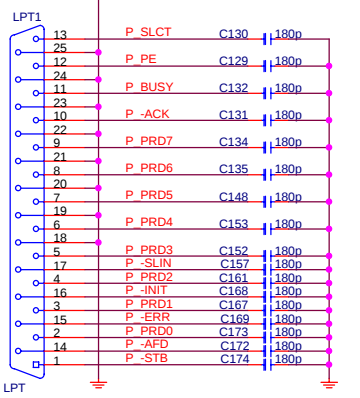


Modification follow requirement of customer

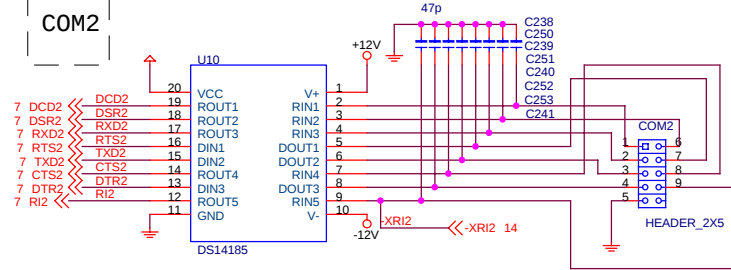
PANEAL1



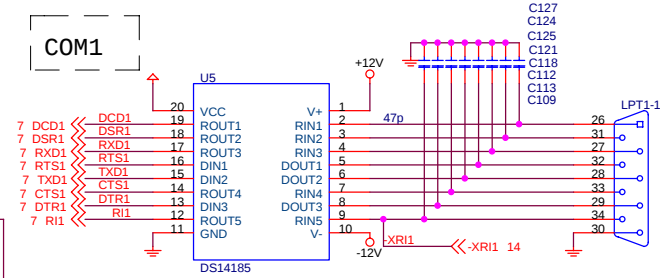
LPT



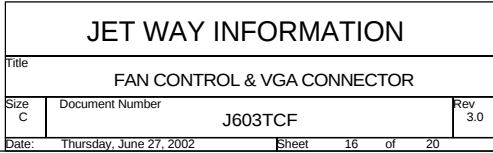
COM2



COM1

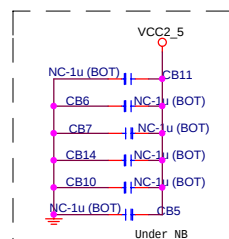


JET WAY INFORMATION			
Title			
FRONT PANEL & BACK PANEL			
Size	Document Number	J603TCF	Rev
C			3.0
Date:	Thursday, June 27, 2002	Sheet	15 of 20

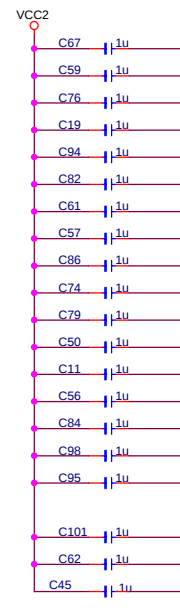
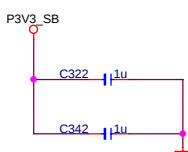
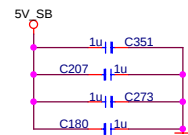
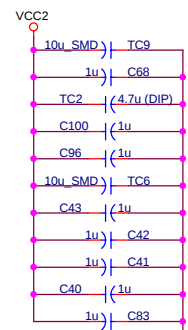
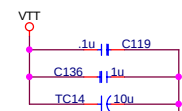
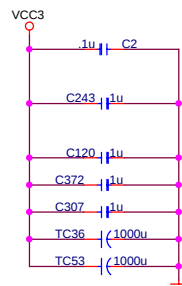


decoupling capacitors for DRAM signals with vias
Place these capacitors near vias

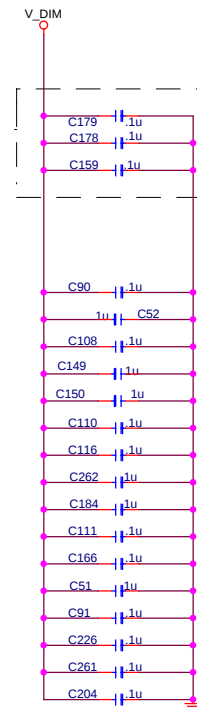
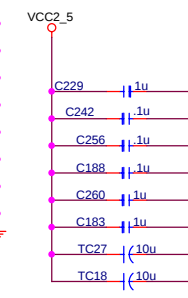
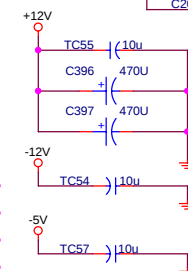
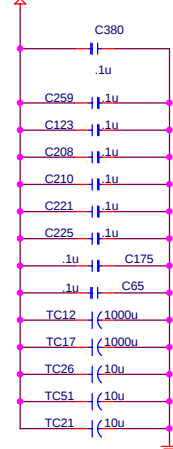
FOR STR FUNCTION



Layout remove 2 VCC3 CAPS



Thomas Hsu Removed VCC TC7 10uF CAP



JET WAY INFORMATION

Title		
ATX POWER/BYPASS CAPACITORS		
Size	Document Number	Rev
C	J603TCF	3.0
Date:	Thursday, June 27, 2002	Sheet 19 of 20

